DESIGN OF POWER AMPLIFIERS USING GaN HEMT

Dissertation submitted to
Visvesvaraya National Institute of Technology, Nagpur
In partial fulfillment of the requirements for the award of the degree

Master of Technology
in
VLSI Design

by

N A AAKAASH KUMARAN
(MT23MVD008)

Under the guidance of

Dr. VASU PULIJALA

Center for VLSI and Nanotechnology
Visvesvaraya National Institute of Technology
Nagpur 440010 (India)

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DECLARATION

I, **N A Aakaash Kumaran**, hereby declare that this dissertation titled "**Design of Power Amplifier using GaN HEMT**" is carried out by me in the **Center for VLSI and Nanotechnology** of Visvesvaraya National Institute of Technology, Nagpur. The work is original and has not been submitted earlier whole or in part for the award of any degree/diploma at this or any other Institution / University.

N A Aakaash Kumaran
Date:

CERTIFICATE

This is to certify that the dissertation titled **"Design of Power Amplifier using GaN HEMT"** is submitted by **N A Aakaash Kumaran (MT23MVD008)** in partial fulfillment of the requirements for the award of **Master of Technology in VLSI Design,** VNIT Nagpur. The work is comprehensive, complete, and fit for final evaluation.

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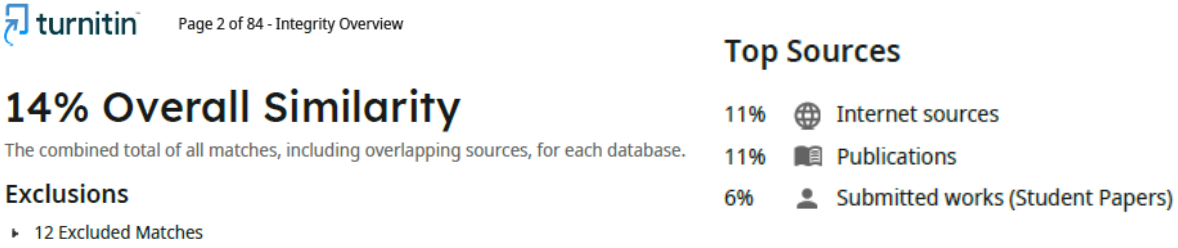

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N A Aakaash Kumaran

ABSTRACT

Power Amplifiers form a critical component in RF transmitter chains, governing the efficiency, output power and signal integrity of wireless communication systems. As modern wireless standards demand higher data rates and extended battery life, the need for compact, high-efficiency amplifiers has become increasingly important – especially in applications like Wi-Fi, where the 2.4 GHz band remains a dominant frequency range. In this context, Class F amplifiers have emerged as an attractive solution due to their potential to significantly enhance efficiency by employing harmonic waveform shaping techniques.

This thesis presents the complete design and simulation of a high-efficiency Class F power amplifier operating at 2.4 GHz, utilizing Gallium Nitride High Electron Mobility Transistor technology. The GaN device is selected for its excellent power density, high electron mobility and robust thermal performance, all of which are crucial for achieving reliable high-power RF output.

The design flow begins with load-line and power estimation, ensuring correct operating conditions for Class F operation. A dedicated biasing network is designed to maintain Class F voltage and current waveforms, while input & output matching networks ensure impedance matching at the fundamental frequency. Harmonic tuning networks are integrated to shape the drain waveforms for reduced conduction loss, a defining feature of Class F PAs. Stability analysis of the complete network is performed to measure and validate unconditional stability. This is followed by PCB layout design where practical considerations are taken into account, and design is validated using simulations.

The methodology and results presented in this thesis offer a practical blueprint for high-performance Class F power amplifier design using GaN HEMTs at microwave frequencies.

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Abbreviations:

RF = Radio Frequency

PA = Power Amplifier

Q-point = Quiescent Point

IMN = Input Matching Network

OMN = Output Matching Network

GaN = Gallium Nitride

GaAs = Gallium Arsenide

SiC = Silicon Carbide

LDMOS FET= Laterally Diffused Metal-Oxide Semiconductor Field Effect Transistor

HEMT = High Electron Mobility Transistor

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1

Introduction

The exponential growth in wireless communication systems has led to an increasing demand for high-performance Radio Frequency (RF) front-end modules. Among these, power amplifiers (PAs) play a critical role in determining the efficiency, linearity, and range of the transmission system. Specifically, in the 2.4 GHz Industrial, Scientific and Medical (ISM) band – commonly used for Wi-Fi and other short-range wireless standards such as IEEE 802.11b/g/n – there is a growing need for compact, energy-efficient and high-power PAs to support the ever-expanding number of connected devices.

While conventional silicon-based technologies have served well in the low- to mid-frequency applications, their limitations in handling high-power densities, wide bandwidths, and thermal constraints become pronounced at microwave frequencies. Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), on the other hand, offer superior electrical and thermal characteristics, such as higher breakdown voltages, high electron mobility and excellent efficiency, making them ideal candidates for RF power amplification in the 2.4 GHz band.

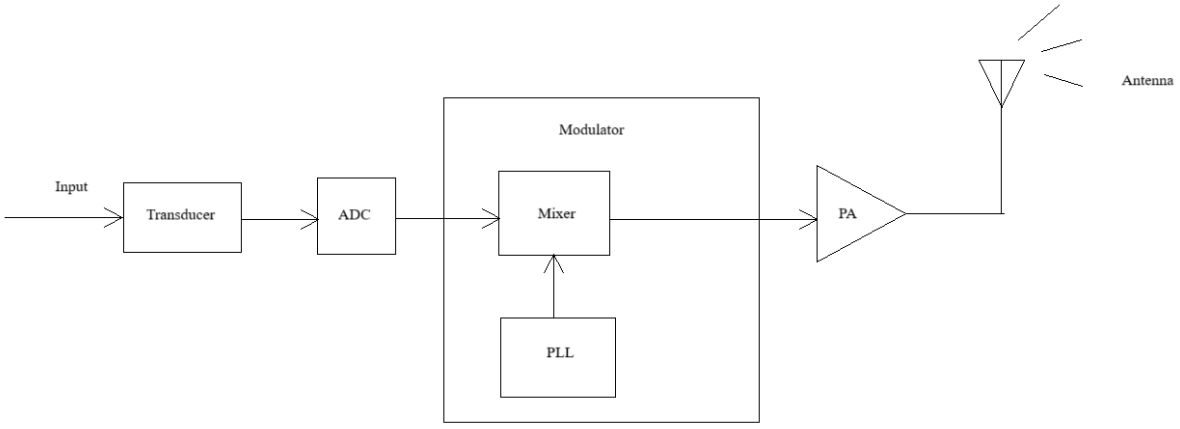


Fig 1.1: Transmitter Block Diagram (Generic)

This thesis focuses on the design, simulation and physical realization of a GaN HEMT based power amplifier targeted for 2.4 GHz Wi-Fi applications. The project aims to achieve a gain of over 20dB, an output power exceeding 35dBm and a notable drain efficiency. The amplifier is designed using a systemic approach that includes schematic simulation, layout

generation, EM co-simulation and PCB fabrication. While the timeline does not permit fill hardware validation before submission, the design has been prepared for fabrication, serving as a practical, fabrication-ready reference for future implementation and testing.

1.1. Motivation

With the Internet of Things (IoT), smart homes and industrial automation driving the need for seamless wireless connectivity, the 2.4GHz spectrum remains one of the most actively used frequency bands worldwide. Ensuring effective coverage and signal integrity in these systems depends heavily on the efficiency and performance of the PA. A well-designed PA can significantly enhance link margin, reduce energy consumption and contribute to thermal management – vital factors in both battery-powered and high-throughput applications.

This project is motivated by the desire to bridge the gap between high-performance simulation-based designs and real-world implementation. GaN HEMT devices offer a compelling opportunity to design compact, reliable and high-power amplifiers with better efficiency and thermal management than their Silicon counterparts. By combining GaN technology with meticulous PCB layout practices and EM simulation, this work aims to develop a practical, fabrication-ready amplifier solution suitable for 2.4 GHz Wi-Fi applications.

The motivation also extends to learning and demonstrating the full design-to-fabrication process, enhancing not only the theoretical understanding but also practical engineering proficiency in RF circuit development.

1.2. Thesis Organisation

This thesis is organized into the following chapters, each building logically upon the previous to present a comprehensive view of the PA design and development process:

Chapter-1: Introduction

Sets the context, introduces the problem and scope, highlights motivation and outlines the thesis flow.

Chapter-2: Literature Review

Presents existing work on PA architectures, GaN HEMT Technology and PCB based realizations to build a foundational understanding and justify design choices.

Chapter-3: Power Amplifiers: Theory, Classes of Operation

Explains the working of Power Amplifiers and their operating classes in depth, the involved trade-offs

Chapter-4: Design Specifications

Defines the design objectives: gain, output power, efficiency, operating frequency, bandwidth and impedance conditions – framed based on literature benchmarks & application needs

Chapter-5: Design Methodology

Presents a systematic approach to designing a Power Amplifier – from biasing and load pull analysis to impedance matching, stability considerations, etc.

Chapter-6: Simulation Setup & Results

Presents the simulation setup utilised for current design and provides results from schematic simulations, highlighting whether the design specs meet the target specs

Chapter-7: Conclusion & Future Scope

Summarizes contributions, reflects on design achievements, limitations and suggests possible extensions to the current design

2

Literature Review

2.1. Introduction

Power Amplifiers (PAs) are critical components in RF Front-end modules, directly influencing the efficiency, linearity and overall performance of wireless communication systems. Among various amplifier classes, Class F PAs have garnered significant attention for their potential to achieve high efficiency through harmonic tuning. This chapter provides an in-depth review of Class F PA Architectures, the advantages of GaN HEMT technology and recent advancements in 2.4 GHz PA designs.

2.2 Class F Power Amplifier Architecture

Class F amplifiers enhance efficiency by shaping voltage and current waveforms through harmonic manipulation. The ideal Class F operation involves:

- **Voltage Waveform:** Square wave achieved by reinforcing odd harmonics
- **Current Waveform:** Half-sinusoidal wave achieved by suppressing even harmonics

This waveform engineering

2.3. GaN HEMT Technology for Class F PAs

Gallium Nitride (GaN High Electron Mobility Transistors (HEMTs) are well-suited for Class F PAs due to their:

- **Wide Bandgap (3.4eV):** Allows high breakdown voltages (>100V)
- **High Electron Mobility (~2000 cm^2/V.s):** Facilitates high-frequency operation
- **High Thermal Conductivity (1.3-1.5 W/cm.K):** Enhances heat dissipation

These properties enable GaN HEMTs to operate efficiently at high power levels and frequencies, making them ideal for 2.4 GHz applications.

2.4. Recent Advances in 2.4 GHz GaN HEMT Class F PAs

Recent research has demonstrated the efficacy of GaN HEMT-based Class F PAs at 2.4 GHz:

Study 1: A 2.4 GHz Class F PA using a 6W GaN HEMT achieved a drain efficiency of 72.8% and a gain of 11 dB at an output power of 40 dBm.

Study 2: A broadband PA operating from 0.6 to 2.4 GHz achieved a maximum drain efficiency of 79.8% with a 10W output using a hybrid continuous Class F mode.

Study 3: A Class F PA designed for WCDMA applications achieved a power-added efficiency (PAE) of 75.8% at 2.14 GHz with an output power of 37.6 dBm using LDMOS technology.

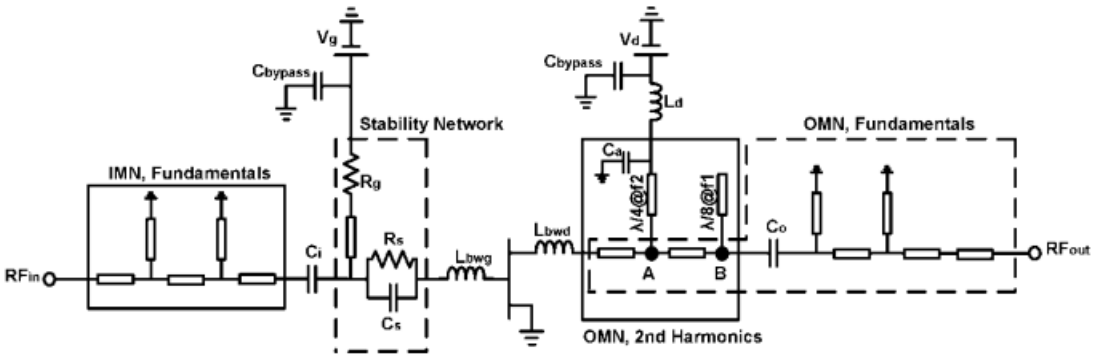


Fig 2.1: Class AB PA from [1]

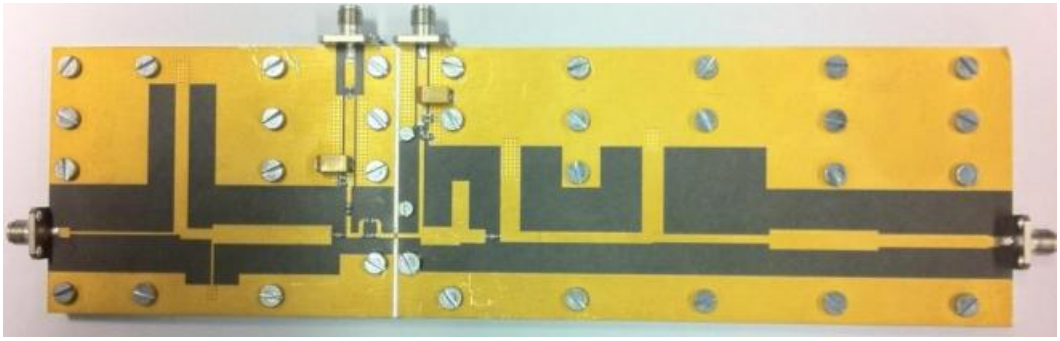


Fig 2.2: Class AB PA PCB from [1]

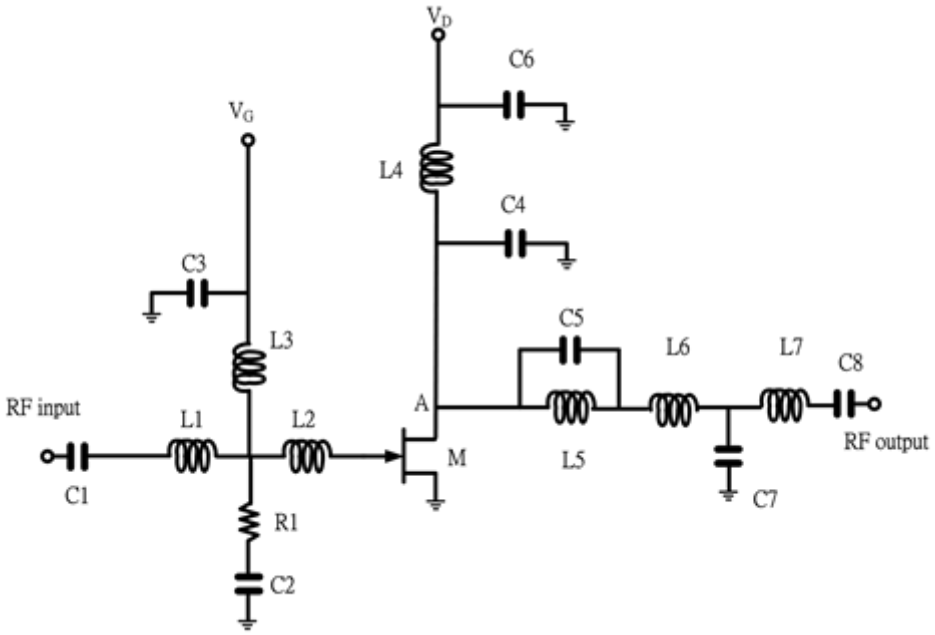


Fig 2.3: Class F schematic from [2]

These studies highlight the potential of Class F architectures in achieving high efficiency and output power at 2.4 GHz.

2.5. Comparative Analysis of Semiconductor Technologies

Semiconductor technology plays a defining role in the performance of RF power amplifiers, influencing efficiency, frequency capability, thermal stability and integration possibilities. While numerous technologies have been employed for RF PA applications, each offers a unique balance of characteristics that make them suitable for specific use cases:

Parameter	GaN HEMT	LDMOS (Si)	GaAs	SiC MESFET
Bandgap (eV)	3.4	1.1	1.43	3.26
Electron Mobility (cm^2/V.s)	~2000	~600	~8500	~1000
Breakdown Voltage (V)	>100	~65	~20	>100
Thermal Conductivity (W/cm.K)	1.3-1.5	1.5	0.46	~4.9
Power Density (W/mm)	5-12	0.7-1	1-2	4-7
Max Frequency	~40+	Up to 4	Up to 100	~10
Efficiency Potential (%)	60-80	45-55	25-35	50-60
Integration Complexity	Moderate	Low	High	Moderate
Typical Applications	Radar, 5G, Satcom, Wi-Fi	Celllular Base-stations, TV Tx	MMICs, low noise RF	Military RF, harsh environment PAs

Table 2.1.: Comparison between Semiconductor technologies for PA Design

2.6. Summary

While all the above technologies are actively used in RF design, GaN HEMTs have recently emerged as the preferred choice for high-power, high-frequency applications due to their combination of wide bandgap, thermal handling and high voltage operation. These attributes are especially advantageous in waveform-based amplifier classes (like Class F) where efficient power delivery depends on rapid voltage and current transitions with minimal loss.

In this work, GaN-on-SiC HEMT Technology is chosen to enable the required performance targets of high-gain, high output power and drain efficiency, in a Class F PA operating at 2.4 GHz.

3

Power Amplifiers: Theory, Classes of Operation

3.1. Introduction

Power Amplifiers (PAs) serve as the final and most critical active block in a RF front-end system. Their primary role is to amplify a low-power modulated RF signal to a high-power level suitable for over-the-air transmission through an antenna. The PA must accomplish this while preserving the fidelity of the signal's envelope and phase, minimizing power consumption and maintaining system stability under various load conditions.

In wireless systems such as Wi-Fi operating at 2.4 GHz, the demands placed on the PA are particularly stringent. These include delivering sufficient output power to ensure link reliability, achieving high efficiency to reduce thermal load and battery drain (in portable devices), and maintaining linearity to limit spectral regrowth in digitally modulated signals.

Designing a PA therefore involves navigating trade-offs between gain, efficiency, linearity, bandwidth and thermal considerations. A thorough understanding of the PA's operating principles and its classification into various conduction modes is essential for selecting an appropriate architecture. This chapter explores the theoretical foundations of PA operation, provides an in-depth explanation of the operating classes and presents the rationale for selecting Class F architecture for this work.

3.2. Operating Principle of Power Amplifiers

At its core, a power amplifier converts DC power from the supply into amplified RF power delivered to a load (typically 50Ω). This conversion is mediated by a nonlinear device – a field-effect transistor (FET) – whose current or voltage response to an input signal is used to generate an enlarged/amplified output signal.

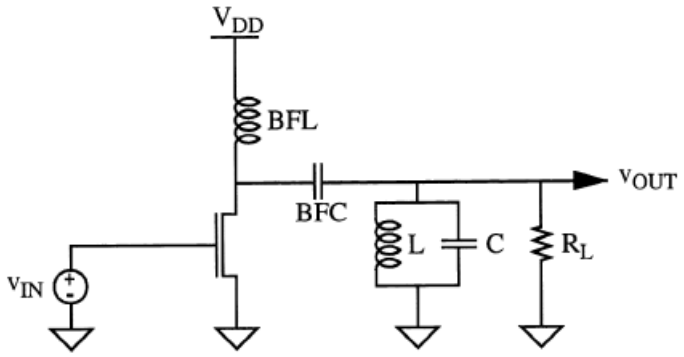


Fig 3.1: Generic PA network [16]

3.2.1. Transistor Biasing and Signal Swing

The operation of the PA begins with biasing the transistor to a specific quiescent operating point (Q-point) on its characteristic curves. This bias determines:

- **Conduction Angle:** The portion of the input RF cycle during which the transistor conducts.
- **Linearity & Efficiency:** Directly impacted by the duration for which the transistor is on or off.

The RF input signal is then superimposed on this bias. As the input varies sinusoidally, the transistor transitions though different regions of operation (cut-off, active, saturation), modulating the voltage in response.

3.2.2. Power Conversion & Matching

Power Gain is achieved by controlling a large current or voltage swing across the output load, and this is maximised when:

- The load impedance is conjugately matched to the transistor's output impedance at the desired frequency
- Matching networks transform 50Ω source/load impedances to the device's optimum load for power, efficiency or linearity.
- Power combining or harmonic tuning is applied where necessary.

Matching networks also serve to filter or shape harmonic content – an essential aspect in non-linear classes like Class F.

3.2.3. Key Performance Parameters

Several metrics define the quality and efficiency of PA operation:

- **Gain (G_P):** the ratio of output to input power (in dB)
- **Output Power (P_{OUT}):** The delivered RF power, often in dBm or watts
- **Drain Efficiency (η):** Ratio of RF output power to DC input power
- **Power-Added Efficiency (PAE):** Indicates how much useful RF power is generated above the input drive level:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \times 100\%$$

- **Linearity:** Preservation of signal envelope, important for modulated signals
- **Stability:** The ability of the PA to resist unwanted oscillations under mismatched or dynamic load conditions

The optimal balance among these parameters is dictated by the class of operation, as discussed below.

3.3. PA: Classes of Operation

Amplifier classes are categorized based on conduction angle -the portion of the input RF cycle during which the transistor conducts current. This angle is determined by the Q-point and directly affects efficiency, linearity and harmonic content.

3.3.1. Class A Amplifier

Class A amplifiers are biased to conduct for the entire 360˚ of the input signal cycle. The transistor operates entirely within its linear region, maintaining faithful reproduction of the input signal at the output.

- **Efficiency:** Theoretical maximum of 50% with a tuned load, though practically 25-35% due to continuous power draw.
- **Linearity:** Excellent, ideal for analog and low-power applications.
- **Applications:** Signal buffering, laboratory instruments, driver stages

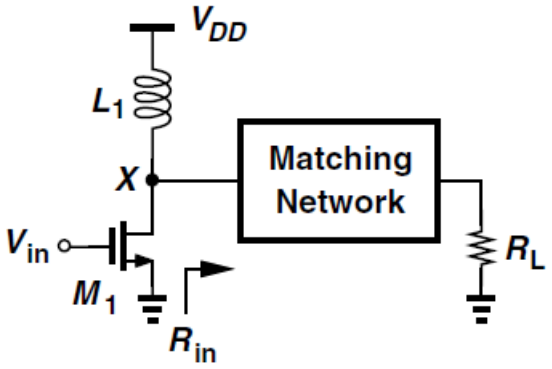


Fig 3.2: Generic Class A PA [14]

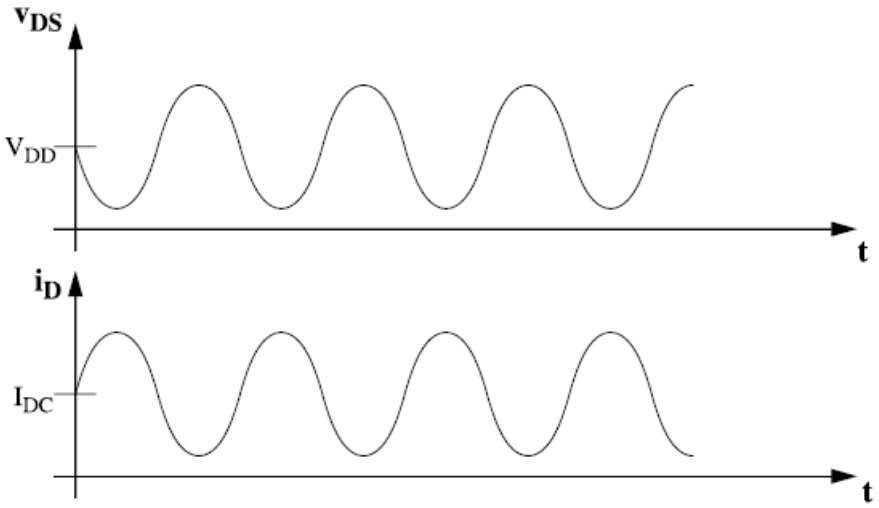


Fig 3.3: Ideal Class A PA I-V waveforms [16]

3.3.2. Class B Amplifier

Here, the transistor is biased at the cut-off point, conducting for exactly 180˚ of the input cycle. To construct the full waveform, Class B amplifiers are usually implemented in push-pull configurations.

- **Efficiency:** Ideally ~78.5%.

- **Linearity:** Affected by crossover distortion near zero crossings.
- **Applications:** Audio systems, older RF transmitters

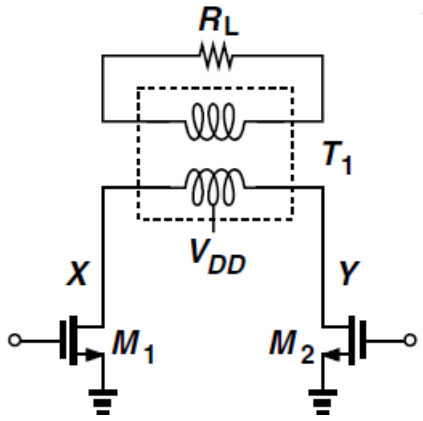


Fig 3.4: Generic Class B push-pull PA [14]

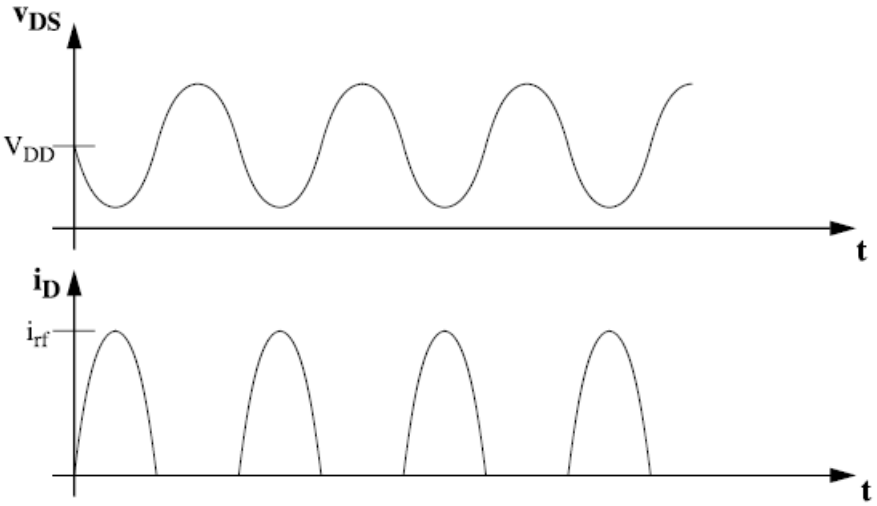


Fig 3.5: Ideal Class B PA I-V waveforms [16]

3.3.3. Class AB Amplifier

Biasing just above cut-off allows conduction for more than 180˚ but less than 360˚, reducing distortion while maintaining better efficiency than Class A.

- **Efficiency:** Typically, 35-60%.
- **Linearity:** Sufficient for communication standards with moderate envelope variation.

- **Applications:** Cellular Base Stations, Wi-Fi PAs, broadcast systems

3.3.4. Class C Amplifier

In Class C operation, the transistor is biased well below cut-off, conducting for less than 180˚. The output contains rich harmonic content and requires a tuned load to recover the desired fundamental frequency.

- **Efficiency:** Often exceeds 70%.
- **Linearity:** Poor, not suitable for amplitude-sensitive modulation.
- **Applications:** Frequency-modulated systems (e.g. FM Transmitters), VCO Drivers

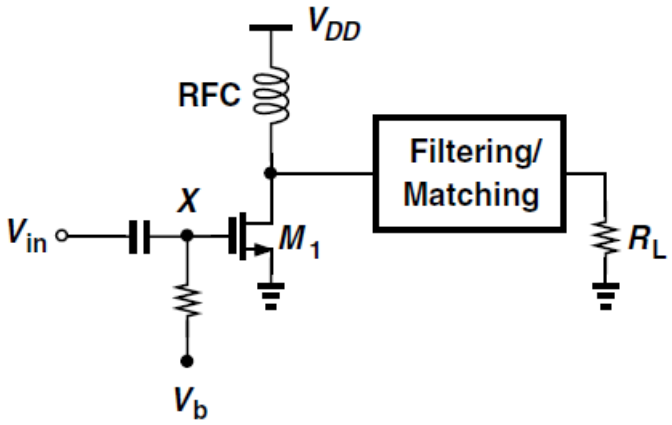


Fig 3.6: Generic Class C PA [14]

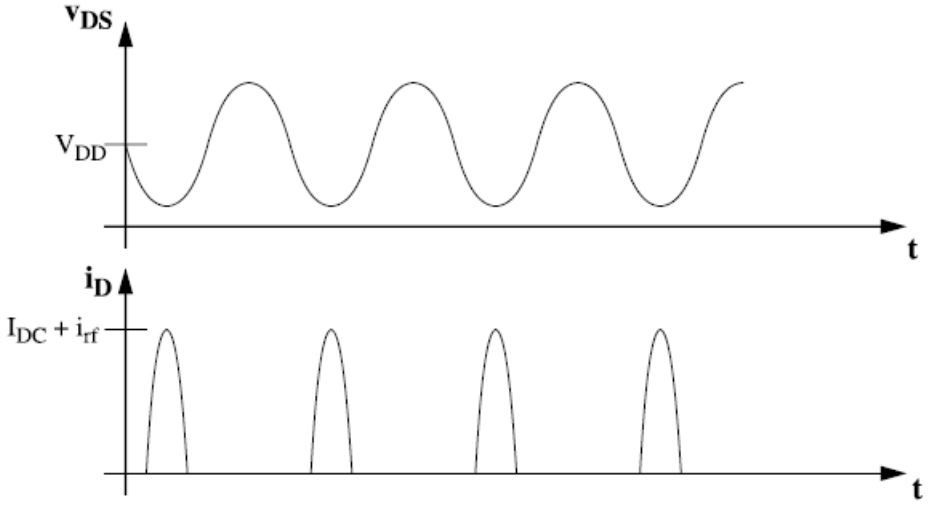


Fig 3.7: Ideal Class C PA I-V waveforms [16]

3.3.5. Class D & E Amplifier

In these configurations, the transistor operates in switching mode, i.e., as a digital switch.

- **Class D:** Utilizes 2 complementary switches driven alternately
- **Class E:** Achieves zero-voltage or zero-current switching to reduce loss
- **Efficiency:** 80-90% achievable.
- **Applications:** Low-frequency power electronics, envelope tracking PAs

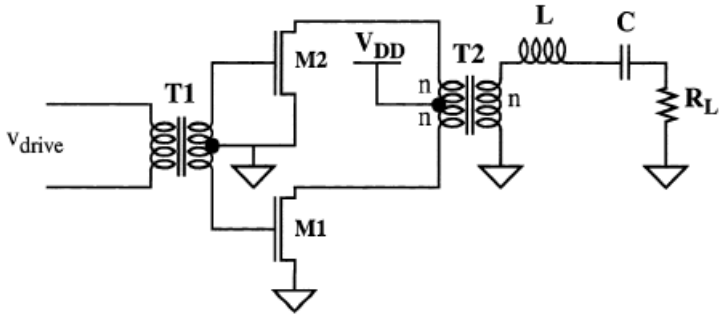


Fig 3.8: Generic Class D push pull PA [14]

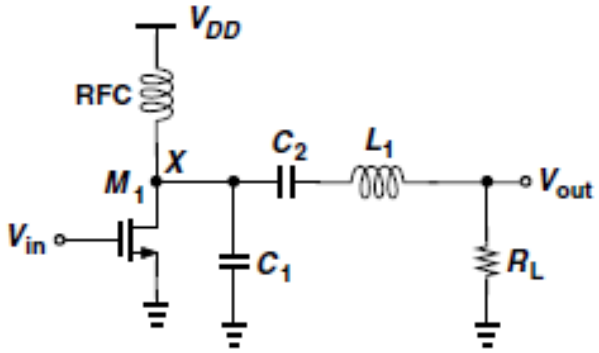


Fig 3.9: Generic Class E PA [14]

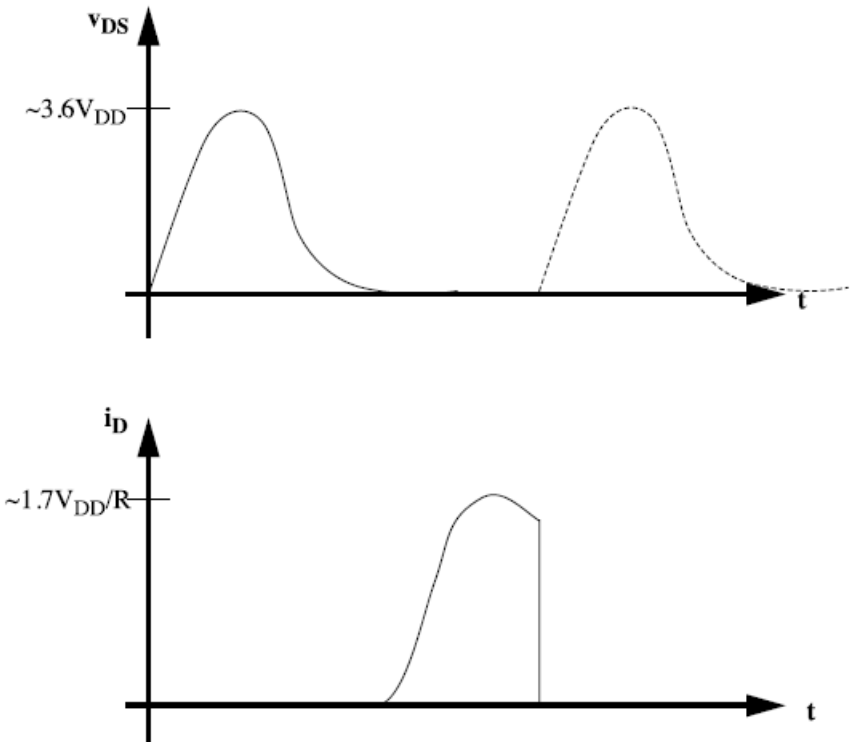


Fig 3.10: Ideal Class E PA I-V waveforms [16]

3.3.6. Class F Amplifier

Class F amplifiers achieve high-efficiency by shaping the waveforms of voltage and current using harmonic tuning networks.

- **Voltage Waveform:** Square-like, achieved by open-circuiting odd harmonics
- **Current Waveform:** Half-sinusoidal, achieved by shorting even harmonics
- This reduces the overlap between high-voltage and high-current, minimizing power loss.
- **Efficiency:** Theoretically > 88%, practically 60-75% with GaN Devices.
- **Applications:** Radar, Wi-Fi, satellite uplinks.
- **Implementation:** Requires harmonic traps or microstrip stubs and careful EM layout optimization

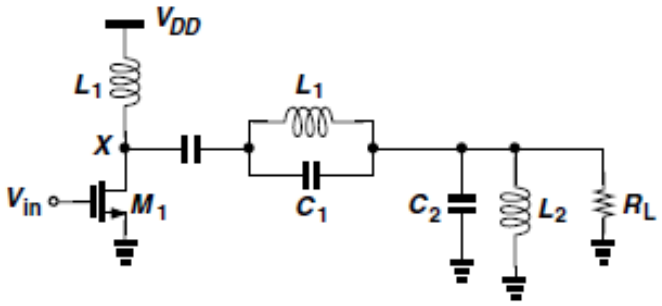


Fig 3.11: Generic Class F PA [14]

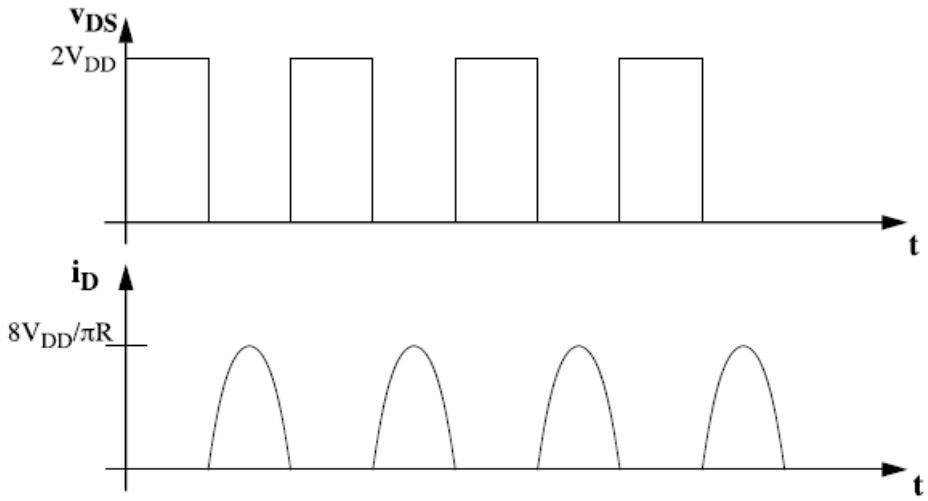


Fig 3.12: Ideal Class F PA I-V waveform [16]

3.4. Summary

Beginning with the operating principles – transistor biasing, impedance matching and waveform shaping – this chapter outlined the distinctions between amplifier classes taking into account their performance parameters.

Special focus was given to Class F, which, through harmonic termination and waveform engineering, offers high efficiency without the need for switching-mode complexity. This makes it especially valuable for 2.4 GHz Wi-Fi applications, where both high output power and acceptable linearity are needed.

With this understanding, the next step is to define the target specifications that the designed amplifier must meet. These include quantitative performance benchmarks derived from system-level demands and device constraints. These specifications will form the foundation for circuit-level design.

4

Design Specifications

4.1. Introduction

In power amplifier design, performance requirements must be clearly established before circuit-level implementation begins. These target specifications define measurable objectives that guide every design decision – from component selection to layout optimization.

For a Class F amplifier designed to operate in the 2.4 GHz ISM band using GaN HEMT Technology, these specifications emerge from a technical evaluation of system-level needs, wireless communication standards and characteristics of the chosen device and architecture. This chapter outlines and explains each specification, placing special emphasis on the significance of each in achieving an efficient & functional RF amplifier for Wi-Fi applications.

4.2. Application: 2.4 GHz Wi-Fi Transmitters

The IEEE 802.11 b/g/n standards define communication in the 2.4 GHz ISM band, with data rates ranging from 1Mbps (802.11b) to over 300 Mbps (802.11n). Wi-Fi transmitters must meet several requirements simultaneously:

- Transmit sufficient power to overcome path losses in both indoor and semi-obstructed outdoor environments
- Efficiency to minimize thermal load, especially in compact or battery-operated devices
- Bandwidth and spectral compliance to support modern modulation schemes like OFDM
- Compatibility with standard test & antenna systems

These application-level constraints directly influence the performance targets for the amplifier presented in this work.

4.3. Key Design Specifications & their Significance

4.3.1. Centre Frequency: 2.4GHz

The amplifier is designed with a centre frequency of 2.4 GHz, placing it toward the lower portion of the ISM band, which spans from 2.4 GHz to 2.4835 GHz. This choice of frequency is a practical design target aligned with channel 1 and adjacent Wi-Fi channels (e.g. 1-6), which are commonly used in real-world networks.

Designing near the lower edge provides a forward margin and allows efficient use of the amplifier over most Wi-Fi allocations. It also simplifies design and simulation when operating within the lower ISM sub-band, especially for fixed frequency or narrow band setups.

4.3.2. Output Power ≥ 35 dBm (3.16W)

An output power level of 35 dBm ensures a string link performance in both indoor and outdoor environments, particularly when used with directional antennas or in development/tests systems.

This level provides headroom above typical Wi-Fi transmitters (20-30 dBm) and allows the amplifier to maintain output even with antenna mismatch or feedline losses.

4.3.3. Power Gain ≥ 20 dB

Typical RF drivers or Wi-Fi transceivers have output signals in the range of 0-10 dBm. A gain of 20dB or more is required to elevate this to the desired output level.

High gain reduces the need for multiple amplifier stages, thereby simplifying design, minimizing power consumption and limiting cumulative phase noise or distortion.

4.3.4. Power-Added Efficiency (PAE) ≥ 60 %

Efficiency is critical in high-power designs to limit heat generation and improve system reliability. A target PAE of at-least 60% is appropriate for Class F

amplifiers using GaN HEMTs, which are well known for their high-efficiency operation due to reduced current-voltage overlap.

Achieving this level of efficiency supports passive cooling and enhances power delivery in thermally constrained systems.

4.3.5. Input & Output Impedance: 50Ω

Designing for 50Ω input and output matching ensures compatibility with:

- Test Equipment (VNAs, spectrum analyzers)
- Standard SMA Connectors and RF Cables
- Antennas and matching networks used in ISM-band hardware

This impedance standard simplifies measurements, reduces mismatch losses and facilitates integration with other RF blocks.

4.3.6. Stability: Unconditional Stability over 0-10 GHz

While the PA is designed for operation at 2.4 GHz, it must be unconditionally stable over a much wider frequency range to avoid oscillations due to load variation, layout parasitics or out-of-band feedback paths.

Ensuring stability from 0-10 GHz accounts for:

- Harmonic resonances up to the 4^{th} Harmonic
- Transient excitation or coupling from adjacent RF systems
- Tuning margin during layout and measurement

Stability is validated using metrics like:

- Rollet's Stability Factor $K > 1$
- Delta $|\Delta| < 1$

This wideband approach guards against unexpected performance degradation or catastrophic failure in field deployments.

4.3.7. Bandwidth ≥ 100 MHz

IEEE 802.11 g/n standards utilize 20-40 MHz channels. A PA bandwidth of atleast 100 MHz guarantees:

- Full coverage of all Wi-Fi channels
- Flat gain and impedance response within the operating band
- Headroom to accommodate layout detuning or EM effects in final hardware

While the amplifier is optimized at 2.4 GHz, this bandwidth ensures its usefulness in adjacent-band experimentation or future tuning.

4.4. Summary of Design Expectations

Parameter	**Target Value**
Centre Frequency	2.4 GHz
Output Power	≥ 35 dBm
Power Gain	≥ 20 dBm
PAE	≥ 60%
Input/Output Impedance	50Ω
Stability	Unconditional, over 0-10 GHz
Bandwidth	≥ 100 MHz

Table 4.1.: Design Expectations Summary

The key performance goals for the 2.4 GHz Class F PA were presented, each of which was anchored in real-world system demands and simulation feasibility. These specifications, while serving as ideal performance metrics, also play an important role as practical constraints that directly shape the amplifier design process.

The next chapter presents the design methodology, detailing how these specifications are translated into schematic-level circuit implementation. Topics include biasing, load-line estimation, impedance matching, harmonic tuning strategies and EM-aware layout planning – all geared toward achieving the performance defined here.

5

Design Methodology

This chapter presents a comprehensive methodology for designing a 2.4 GHz Class F RF Power Amplifier using GaN HEMT Technology.

5.1. Overview of Design Flow

The following diagram helps visualize the complete flow of the design process:

5.2. Active Device Selection & Modelling

The transistor or active device forms the core of the power amplifier. The chosen device must meet the performance needs such as frequency range, power level, gain and efficiency.

- **Selected Device:** GaN HEMT
- **Key Features:** High breakdown voltage, high electron mobility, high power density, suitable for high-efficiency operations such as Class F

The non-linear model provided by the manufacturer is imported into the simulation environment (in this work, Keysight ADS). This model is validated by comparing simulated I-V characteristics with datasheet curves.

5.3. Bias Point Selection

The bias point defines the static operating conditions of the transistor before any RF signal is applied. Choosing an optimal bias point is critical because it influences:

- Linearity
- Conduction Angle
- DC Power Consumption
- Dynamic Range & thermal stability

For Class F operation, which aims to shape the current and voltage waveforms for minimal overlap, a bias close to Class B is generally used. This corresponds to a conduction angle of 180˚, providing high efficiency.

5.3.1. Determining the Bias point

V_{DSQ} (Drain-Source Voltage):

- Chosen as 70-80% of the transistor's breakdown voltage
- Example: For a 50V GaN Device, V_{DSQ} ~ 30-35V

I_{DQ} (Quiescent Drain Current):

- For Class F, lightly biasing with I_{DQ} typically 5-20% of I_{max}
- A typical value may be 50-100 mA depending on the device

5.3.2. Implementing the Bias

- Gate bias is supplied through a high value resistor or RF choke.
- Drain bias is fed through a broadband RF choke with bypass capacitors to maintain a clean DC supply.

DC block capacitors are inserted at the RF input and output to prevent DC bias from interfering with other stages.

5.4. Load Line & Output Power Estimation

The load line helps determine how the transistor transitions between cut-off and saturation when amplifying a signal. Drawing the load line on the transistor's I-V curves allows you to estimate output power and identify safe operating conditions.

5.4.1. Calculating Load Line parameters

Voltage Swing (V_{DS}): The maximum voltage swing is typically chosen as 70-80% of the breakdown voltage

Current Swing (I_D): Estimated based on the desired output power using the formula:

$$P_{OUT} = \frac{1}{2} V_{swing} \times I_{swing} \times \eta$$

5.4.1. Calculating Optimum load impedance

Once voltage and current swings are known:

$$Z_{opt} = \frac{V_{swing}}{I_{swing}}$$

This complex impedance becomes the goal for the output matching network.

When using a simulator, Z_{opt} can be obtained empirically by using Load-pull simulations, where load impedances are swept and P_{OUT} and PAE are measured. This will give the optimal source and load impedances for the transistor chosen for both maximum efficiency and maximum power output, and we can make a decision to select either of the 2 sets of impedances, based on our application requirements.

5.5. Biasing Network Design

In RF power amplifiers, proper biasing ensures the active device operates in the desired class (Class A, AB, B, F, etc.) with thermal and DC stability. For this Class F amplifier using GaN HEMT device, biasing is particularly important due to high voltage swing and need for harmonic control.

Key Considerations:

- Class F operation ideally requires a quiescent current neat Class B (around 10-15% of I_{max}) with voltage swing shaping handled by harmonic tuning.
- GaN HEMTs are normally off, requiring a negative gate bias (V_{GS}) to turn on and positive drain bias (V_{DS}) for power delivery.

Bias Network components:

- **RF chokes (high impedance at RF):** Prevent RF leakage into DC supply

- **Decoupling capacitors:** Short high-frequency noise to the ground, ensuring stability
- **Resistors (optional):** In gate bias to avoid oscillations or for current sensing

A sequencing circuit may be required in hardware to ensure gate bias is applied before drain bias to prevent device damage. In simulations, ideal DC sources are used with sequencing assumed to be externally managed.

5.6. Matching Network Design

Matching networks are used to maximize power transfer and control harmonic terminations. They are implemented using microstrip transmission lines, capacitors, or stubs.

5.6.1 Input Matching

The input impedance of the transistor at 2.4 GHz is generally complex and mismatched with the 50Ω source. Using the Smith chart, the required input matching network (IMN) can be determined:

- From load-pull simulation, the target input impedance for maximum power output, Z_{in} is extracted
- The matching network is then designed to convert 50Ω to Z_{in}.

When using a simulator like Keysight ADS, the Smith chart tool can be used to plot the source and load impedances on the Smith chart, and add the desired components in the required configuration (π-network, T-network, etc.) using lumped or distributed components, which lead the impedance path from load to source impedance on the Smith Chart. This will give the values for the components involved, which can then be used to verify the match using a schematic testbench, involving a S-parameter analysis.

5.6.2. Output Matching

The output matching network (OMN) must:

- Match the transistor's optimal load impedance (Z_{opt}) for fundamental frequency power delivery.
- Provide short/open terminations at 2nd & 3rd harmonics for Class F operation.

From Load-Pull Simulation results, Z_{opt} is identified for maximum output power. Then:

- A fundamental matching network is designed from Z_{opt} to 50Ω.
- For harmonic control, short-circuited stubs ($\lambda/4$ at $2f_o$) and open circuited stubs ($\lambda/4$ at $3f_o$) are added near the drain to reflect harmonics constructively.

As done for IMN Design, Smith chart can be used here similarly. The stubs involved for harmonic tuning can be added to the smith chart and verified that they do not impact the impedance matching significantly.

Harmonic balance simulations in ADS are used as a next step to verify the voltage/current waveforms and harmonic impedances.

5.7. Harmonic Tuning for Class F Operation

Class F amplifiers use harmonic termination to shape the drain waveform into a square voltage and half-sinusoidal current for maximum efficiency. Theoretically,

- Voltage waveform includes only odd harmonics
- Current waveform includes only fundamental (ideally)

Implementation:

- **2nd Harmonic Short Stub ($\lambda/4$ open stub at $f = 2f_o$):** Transforms to short at transistor drain

- **3rd Harmonic Open Stub ($\lambda/4$ shorted stub at $f = 3f_o$):** Transforms to open at transistor drain

These stubs are placed strategically within the OMN layout, with spacing adjusted to maintain effective harmonic impedance transformation.

Harmonic Balance simulation in ADS confirms:

- Drain voltage waveform ~ Square Wave
- Drain current waveform ~ Sine wave

This ensures Class F behaviour is achieved.

5.8. Stability Analysis & Compensation

GaN PAs, due to their high gain and wide bandwidth, can be prone to oscillations unless explicitly stabilized.

5.8.1. Stability Assessment:

To ensure unconditional stability across the complete frequency range:

- Rollet's Stability Factor (K-factor): Must be $K > 1$
- Delta (Δ): Must be $|\Delta| < 1$
- Stability Circles: Plotted on the smith chart to visualize unstable regions (for unconditional stability, these circles must not be inside or touch the boundaries of the smith chart – implying that for any impedance, the network is stable)

Simulations using ADS with S-parameter sweeps in the desired frequency range can help locate any frequency regions which do not satisfy the above conditions.

5.8.2. Stabilization Techniques:

If instabilities are observed:

- Gate resistors (~2-10Ω): Dampen low-frequency oscillations
- Shunt RC Networks: Placed at output to control high-frequency ringing

- Broadband decoupling: Prevent feedback via power lines

Once any of the above techniques are utilized and, stability can be verified using S-parameter simulations, plotting the stability circles and verifying K-factor and Δ values.

5.9. PCB Layout Design Methodology

The PCB layout process translates schematic designs into physical form while preserving RF behaviour, controlling parasitics and ensuring thermal/mechanical integrity.

5.9.1. Substrate & Stack-up selection:

- Substrate: 0.3mm FR4 with $\varepsilon_r \approx 4.4$, loss tangent ~0.02. This is suitable for low-cost prototyping despite limitations at 2.4 GHz
- Stack-up: 2-layer design, with top layer holding the design and bottom layer as a continuous ground plane, with via stitching

5.9.2. Microstrip Line Sizing:

Using ADS LineCalc, trace widths for 50Ω can be computed, keeping in mind:

- Width adjustments made for high-current drain lines
- Substrate and Conductor thickness decided and given as input

5.9.3. Harmonic Stub & Matching Layout:

Implementation:

- Straight Stubs can be used – microstrip lines kept open, or shorted to ground representing open/short stubs
- They can be connected using T-junctions
- Spacing should be optimized to avoid mutual coupling

5.9.4. Parasitic Management and Layout Best Practices:

PCB layout introduces stray capacitance, inductance and ground return issues, which must be carefully mitigated. The following guidelines are to be followed:

- Short RF paths: To minimize parasitic inductance

- Wide Drain lines: To reduce IR Drop and improve power handling
- Tapers: Used to connect wide traces to narrow SMD pads (length ≥ 3 times width difference for smooth impedance transition)
- RF and DC lines spaced well apart to prevent interference

DRC Management:

- Constraint rules in Cadence Allegro/Keysight ADS adjusted to allow larger traces and tighter component spacing
- Custom clearance rules can be defined for RF regions

Parasitic Validation:

- EM Simulation of layout done using ADS momentum simulator
- Deviations (if any) can be observed and necessary corrections can be made

5.9.5. Decoupling & grounding strategy:

- Capacitor Banks: Placed on Bias lines, will ground any RF noise coming in from the DC source
- Via Stitching: Every 1-2mm to reduce any loop inductance
- Ground-pour: Continuous under RF lines, except near stub terminations to avoid shorting intended circuits.
- Independent RF and DC Grounds: To avoid DC bias corruption by noise due to RF signal interference in return path

5.9.6. RF Connectors & DC feed integration:

- SMA Connectors: Aligned with 50Ω matched microstrip transitions
- DC Coaxial Jacks: Added for Gate and Drain bias, routed away from RF paths
- Chokes and isolation components: Prevent RF coupling into DC lines.

5.10. EM Co-simulation Setup

Post-layout performance validation is essential, as physical effects can alter matching and harmonic tuning.

5.10.1. EM Model Extraction:

- ADS Momentum is used to simulate PCB Layout and extract an EM model
- Define ports at SMA, bias inputs, transistor pads and component locations
- Substrate properties and metal layers matched to real PCB

5.10.2. Co-Simulation Flow:

- Create symbol for EM model
- Integrate in schematic with lumped elements
- Run Co-simulation to extract:
    - S-parameters
    - Output Power
    - Gain & PAE
    - Harmonic content

Comparison with schematic-only results will reveal any deviations. If the differences are minor, it indicates a robust layout integrity.

5.10.3. Significance of Co-Simulation:

- Accounts for stub detuning, parasitics and pad-effects
- Verifies correct harmonic termination post-layout
- As a final step before fabrication ensures a high confidence in board performance

5.11. Summary

A comprehensive methodology for approaching the design of a high-efficiency Class F PA is presented. We considered the theoretical parameters, the design process involved and the practical implementation points as a part of the end-to-end design flow.

Key layout strategies were discussed in depth to address parasitics and practical implementation challenges. This was followed by EM simulation and co-simulation techniques to validate the layout and ensure the desired performance.

The next chapter will present the simulation setup, obtained results and performance evaluation, including the harmonic balance analysis, power gain, output power, efficiency along-with a discussion on how well the design meets the target specifications outlined earlier.

6

Simulation Setup & Results

This chapter presents the simulation methodologies adopted, the tools used and detailed analysis of the designed Class F PA using Qorvo's QPD0030 GaN HEMT. Simulation steps span from device-level characterization to full-circuit and layout-based validation. The EDA tool used for all the simulations and analyses performed is Keysight Advanced Design System (ADS).

6.1. Device Stability Analysis

Before initiating any network level design, the selected GaN HEMT was initially analysed for stability across a wide frequency range (0-10 GHz). The below setup was used:

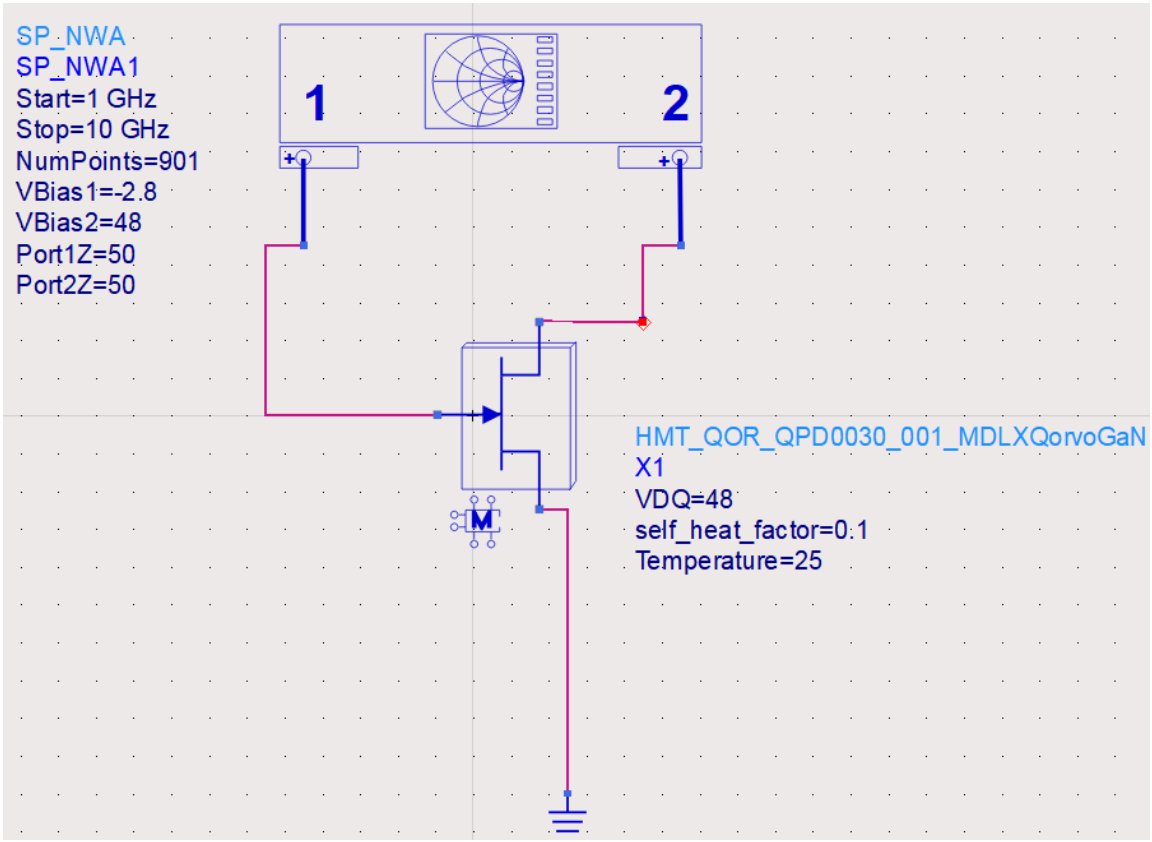


Fig 6.1: Stability Analysis – isolated HEMT

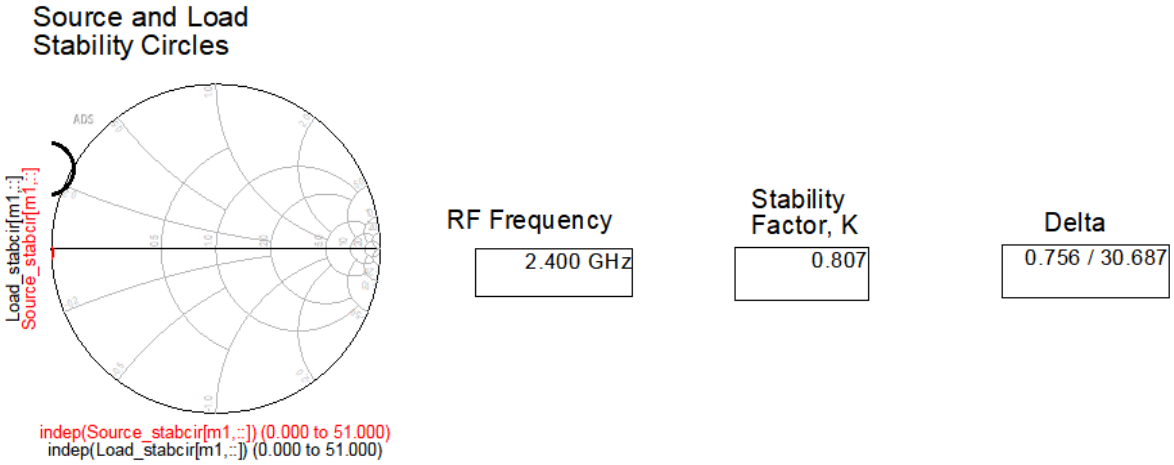


Fig 6.2: Results showing instability

Observing the instability of the HEMT in isolation, a series resistor was added at the gate and its value was optimized to get a K value as just above 1 and $|\Delta| < 1$. Using a higher value of resistor leads to a higher K, but the inherent gain offered by the transistor was observed to reduce. Hence, the below setup was arrived at which provides a good gain without any major deviations and assures unconditional stability over the selected frequency range:

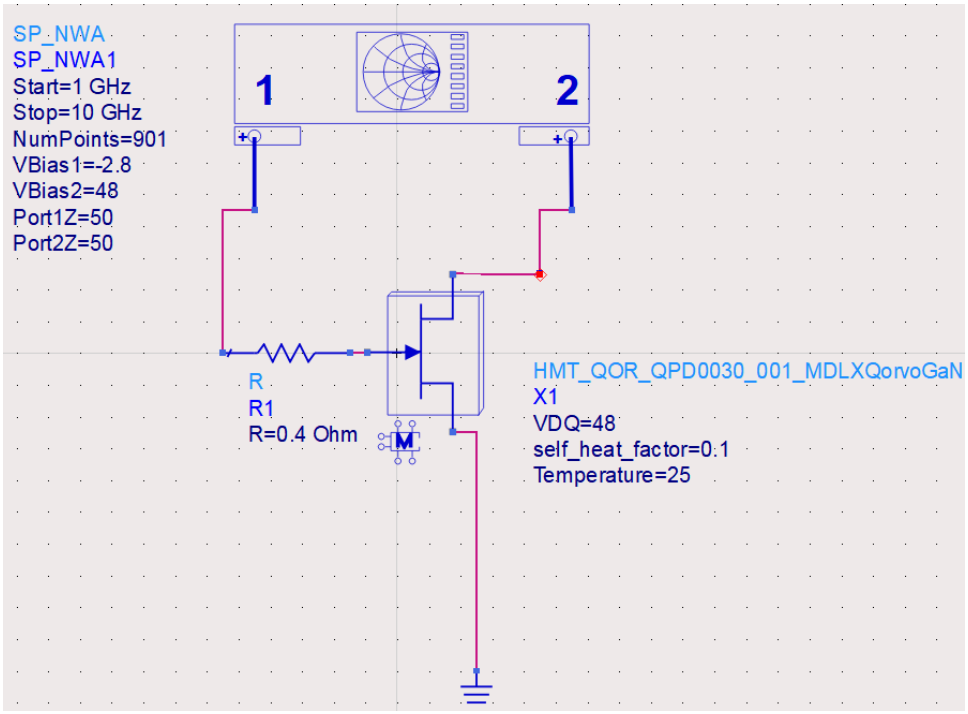


Fig 6.3: Stability Analysis – Modified setup for unconditional stability

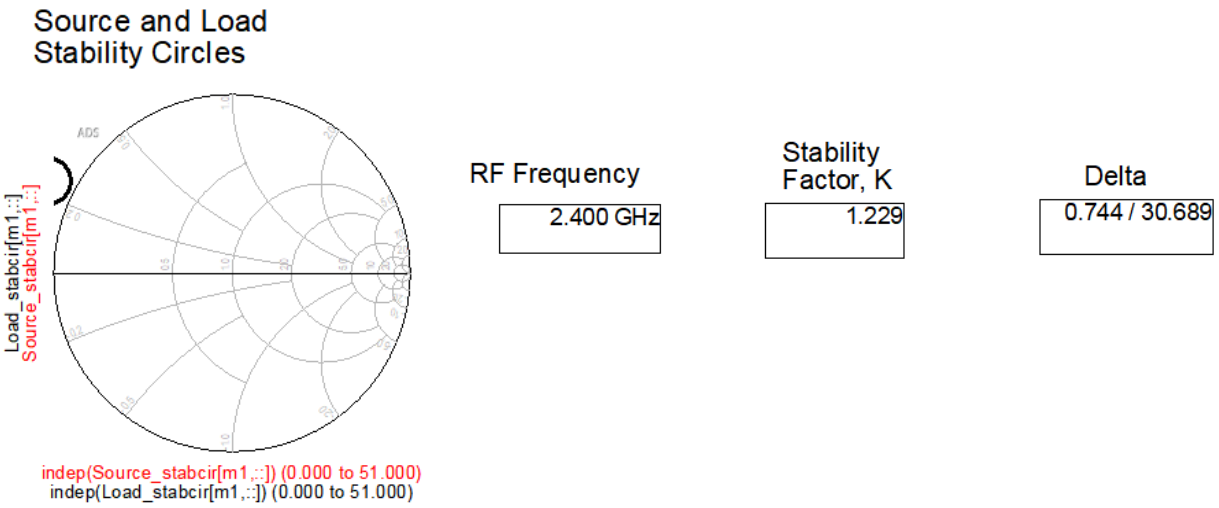


Fig 6.4: Results validating unconditional stability

6.2. Load Pull Simulation

As a next step, a large signal load pull analysis was conducted at 2.4 GHz to identify the optimum source and load impedances for maximum power output. The setup used is as below:

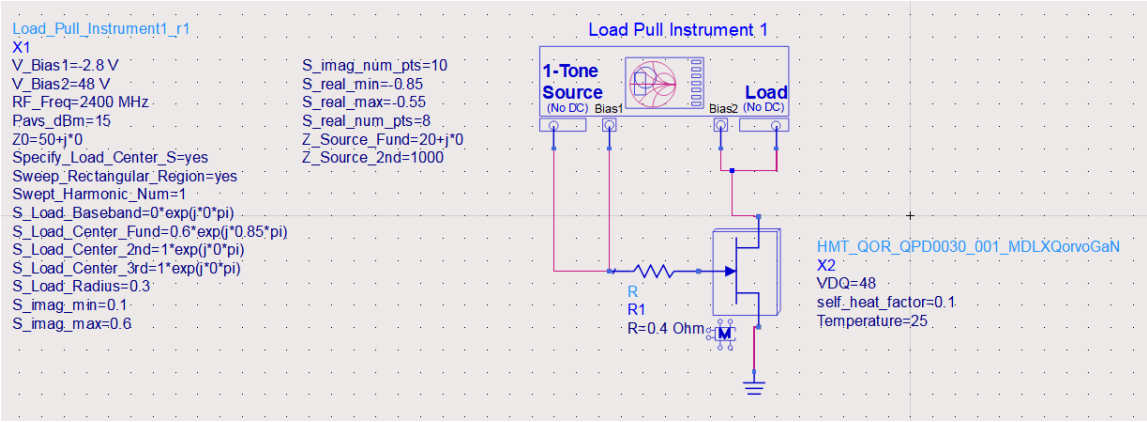


Fig 6.5: Load Pull Setup for QPD0030

The below results were obtained:

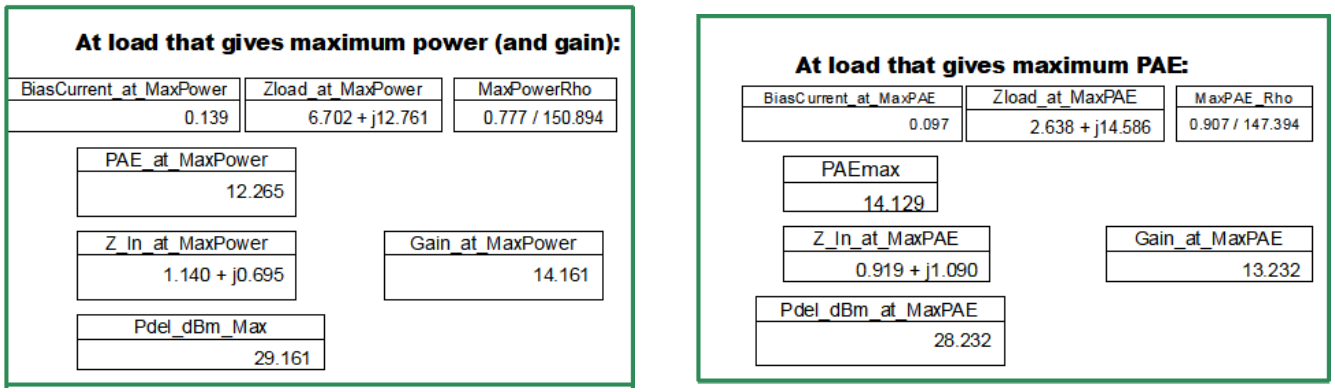


Fig 6.6: Load Pull Results – Maximum Power & Maximum PAE

Now, the above optimized source and load impedance values are taken for design of matching networks.

6.3. Input Matching Network (IMN) Design

The IMN was designed using a Smith chart based approach to transform a 50Ω source impedance to the complex conjugate of $Z_{in_{opt}}$ at 2.4 GHz. The Smith Chart Utility in Keysight ADS was used for this purpose. The harmonic tuning network was added on the input side too to shape the waveforms received from the RF input

The below image shows the matching network designed in the smith chart tool:

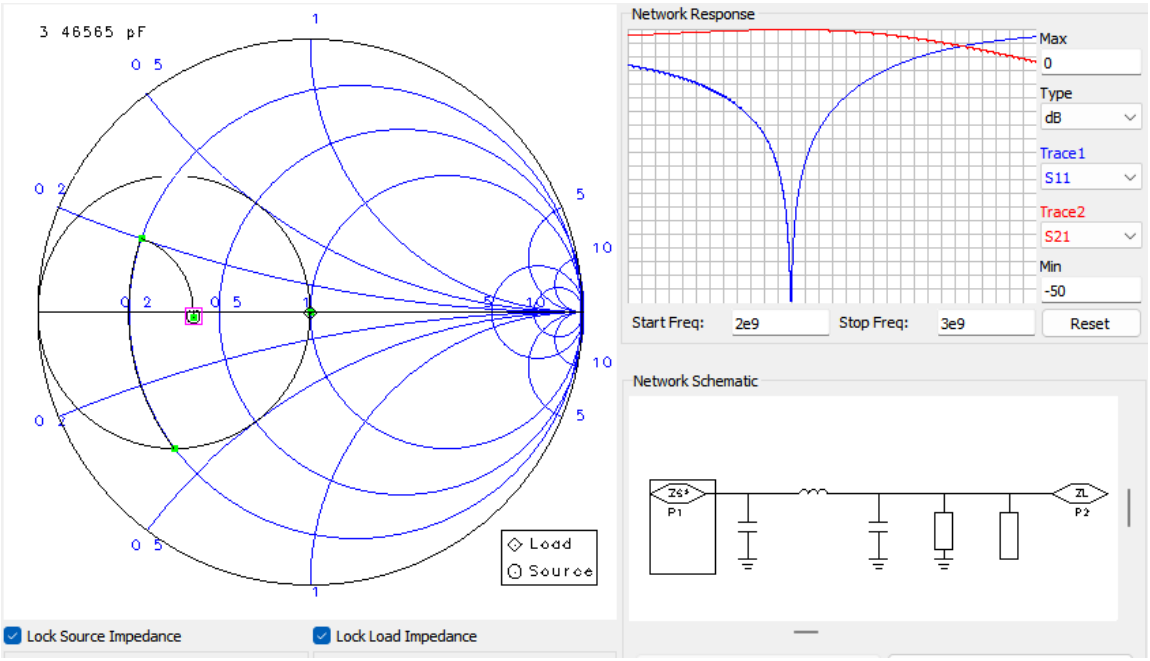


Fig 6.7: Smith Chart Setup for IMN Design

The below setup was subsequently used to validate the design's performance by running a S-parameter analysis:

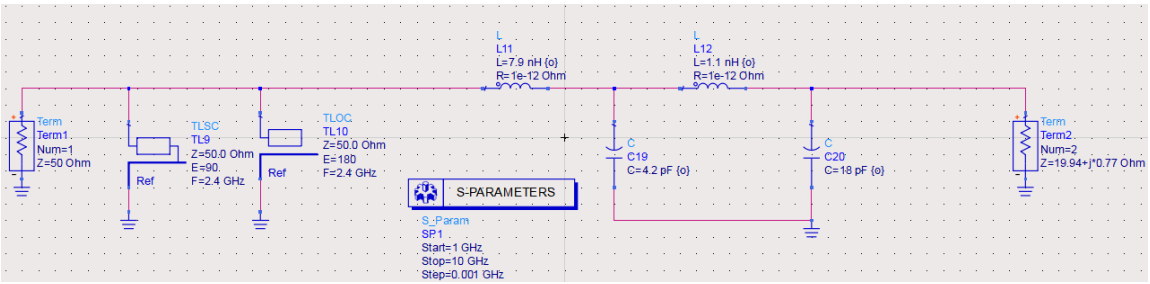


Fig 6.8: S-parameter analysis setup for IMN

The results of S-parameter analysis was obtained as follows:

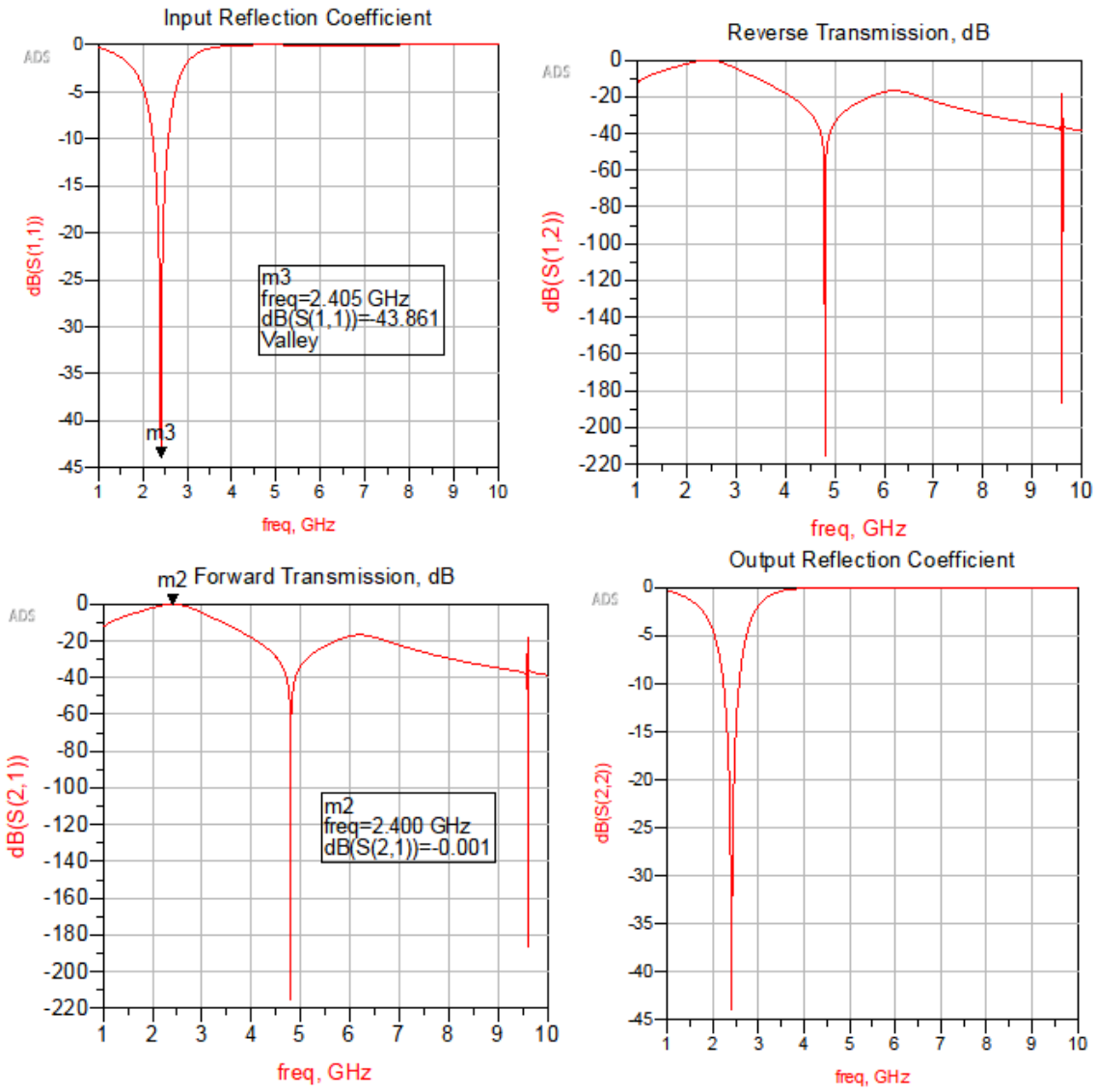


Fig 6.9: S-parameter Results for initial IMN Design

6.4. Output Matching Network (OMN) & Harmonic Termination

The OMN was designed using a Smith chart based approach to transform a 50Ω source impedance to the complex conjugate of $Z_{load_{opt}}$ at 2.4 GHz and to incorporate harmonic termination. The Smith Chart Utility in Keysight ADS was used for this purpose. $\lambda/4$ and $\lambda/2$ stubs were used to create a short and open at $2f_o$ and $3f_o$ respectively.

The below image shows the matching network designed in the smith chart tool:

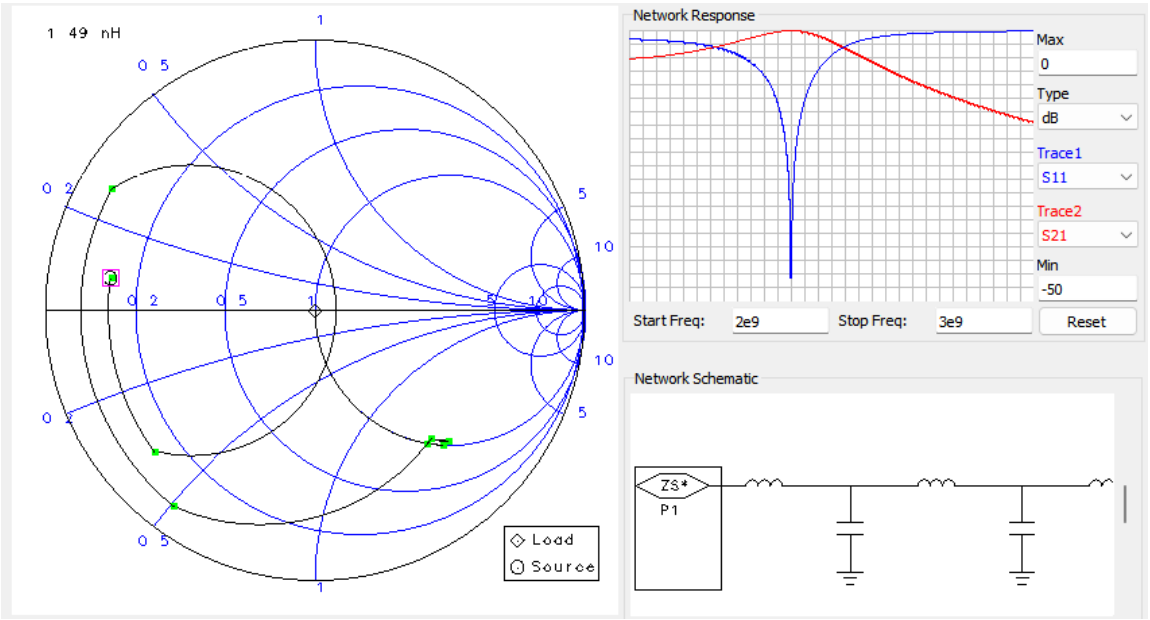


Fig 6.10: Smith Chart Setup for OMN Design

The below setup was subsequently used to validate the design's performance by running a S-parameter analysis:

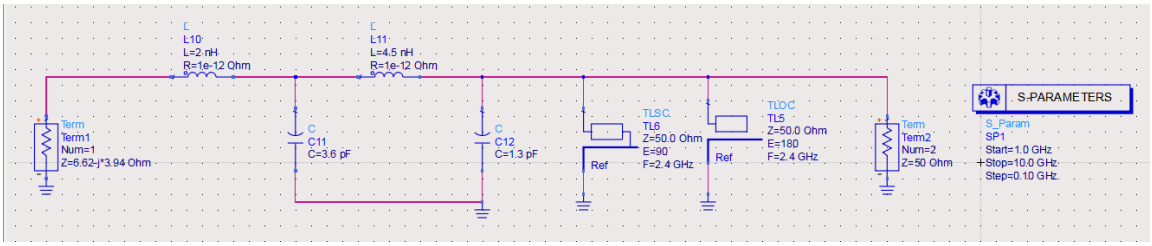


Fig 6.11: S-parameter analysis setup for initial OMN

The results of S-parameter analysis was obtained as follows:

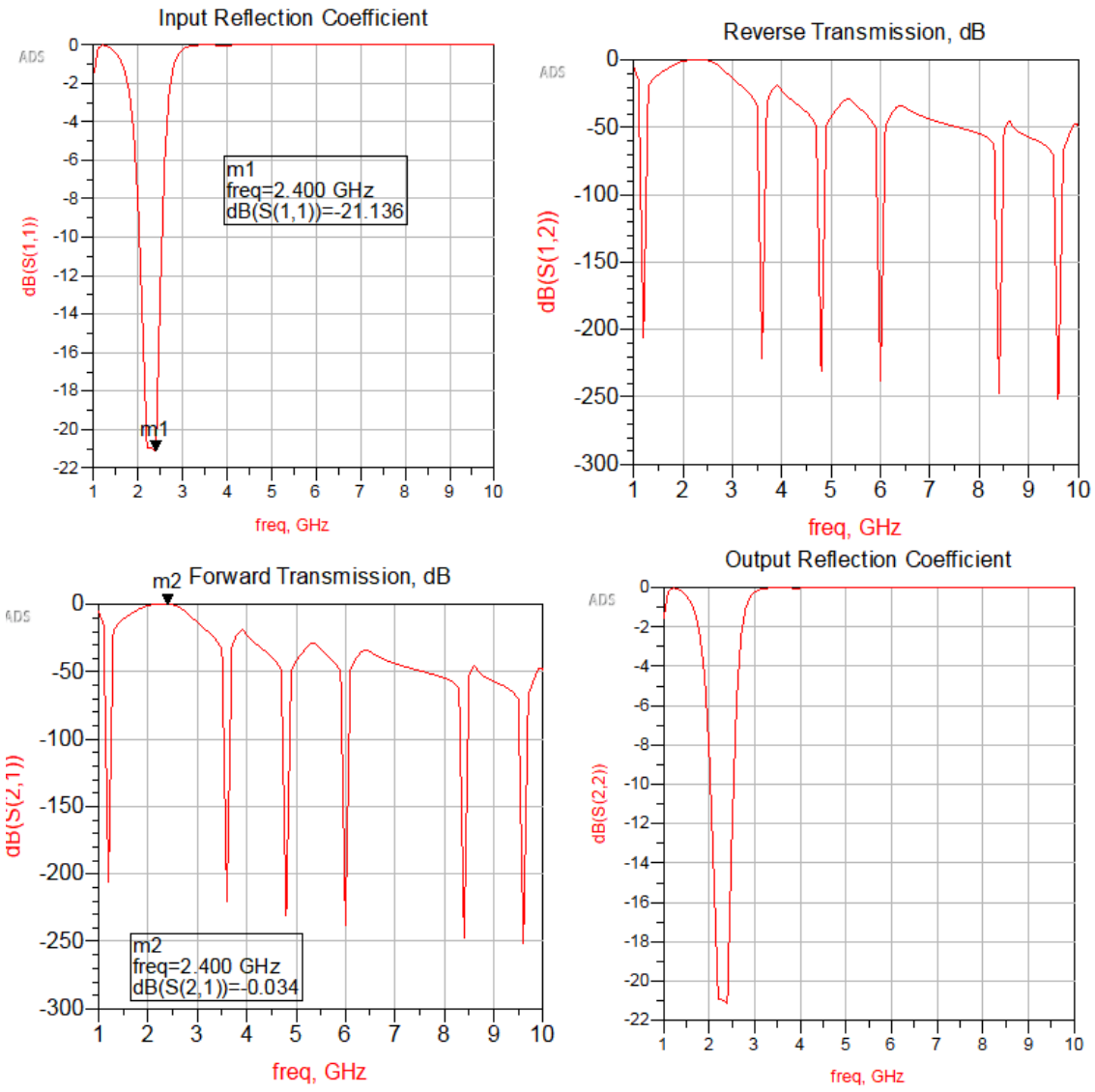


Fig 6.12: S-parameter Results for initial OMN Design

6.5. Overall Network Stability

After combining IMN and OMN, along with their respective harmonic tuning circuits, the overall network stability was reassessed using the below setup:

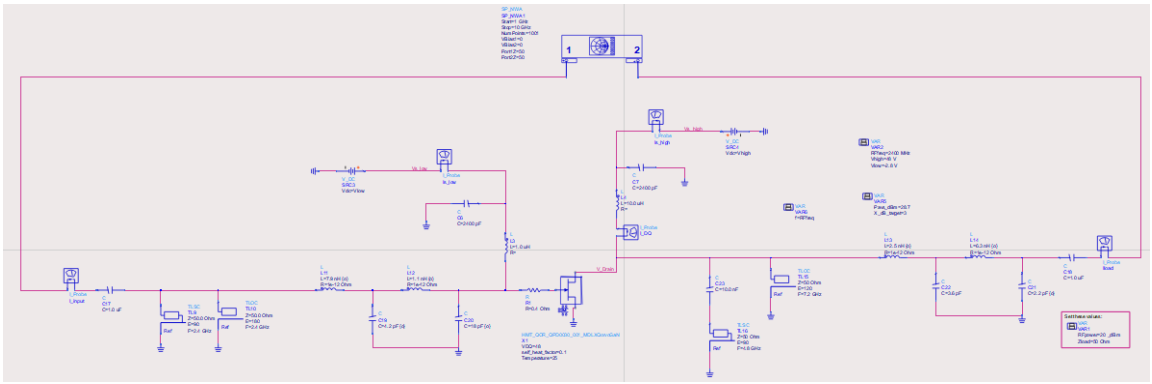


Fig 6.13: Setup for overall network stability analysis

The complete amplifier network remained unconditionally stable, with stability circles confirming acceptable source/load regions, as shown below:

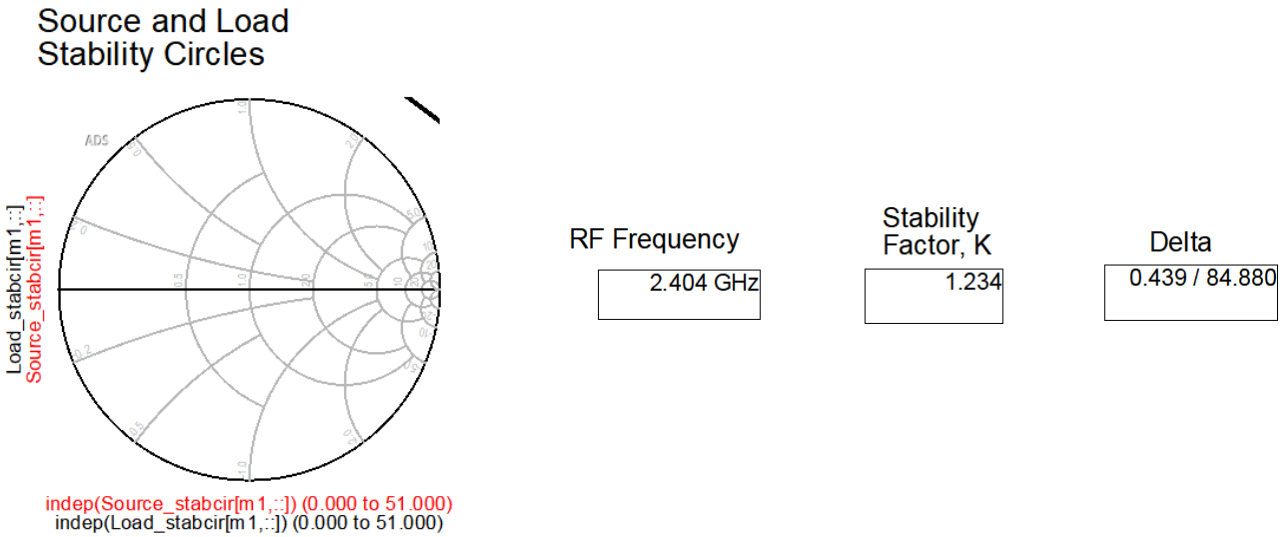
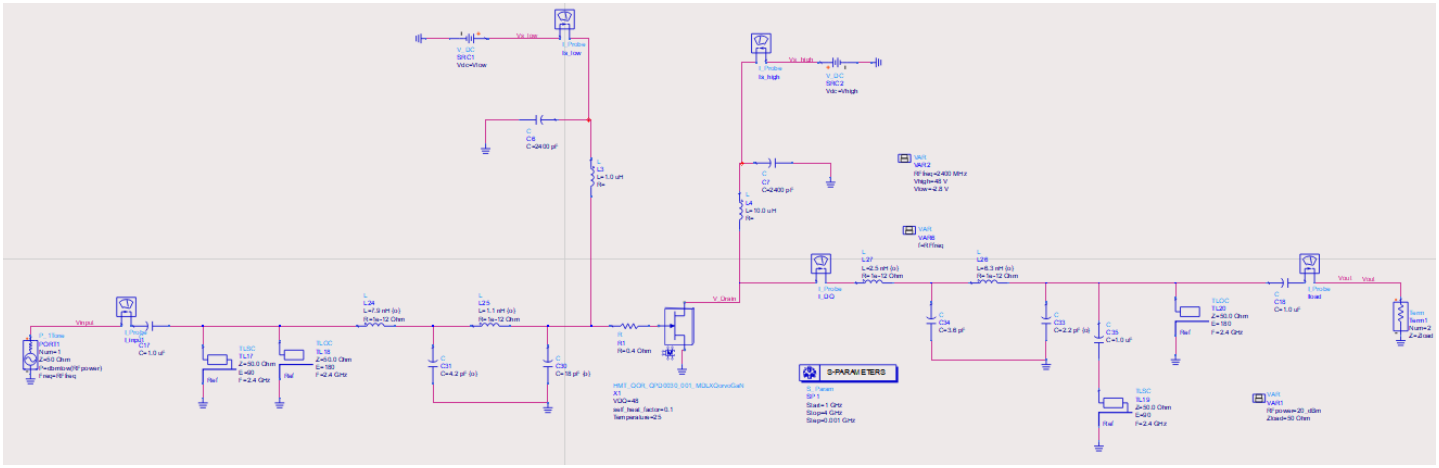


Fig 6.14: Stability analysis results – overall network

6.6. S-Parameter Analysis

Small Signal S-parameters were simulated from 0 to 10 GHz to observe the overall network performance, using the below setup:



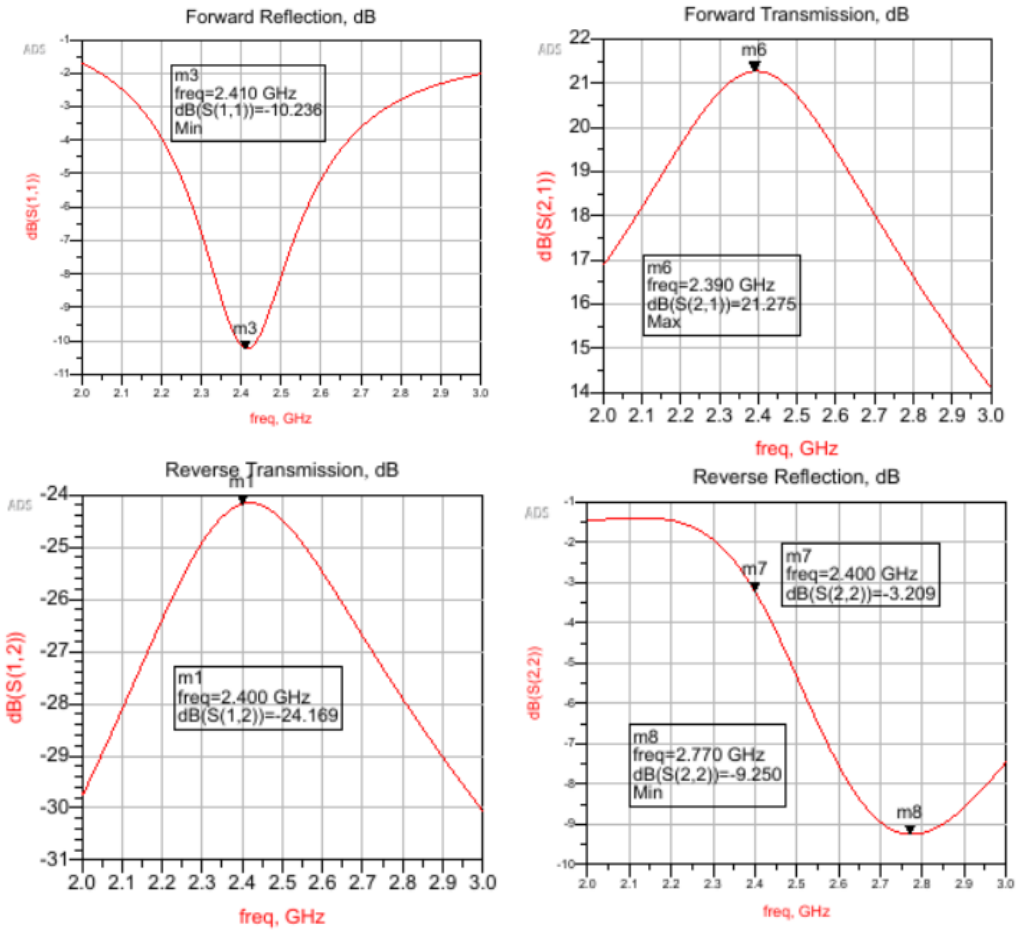


Fig 6.15: S-parameter Analysis setup & results for overall initial network

- S_{11} < -10dB at 2.4 GHz, implying a good input match

- S_{21} > 20dB, showing a good transmission gain
- S_{22} moderately low, indicating sufficient output match.

6.7. Harmonic Balance Analysis

HB Simulation was employed to assess non-linear behaviour of the amplifier, using the below setup:

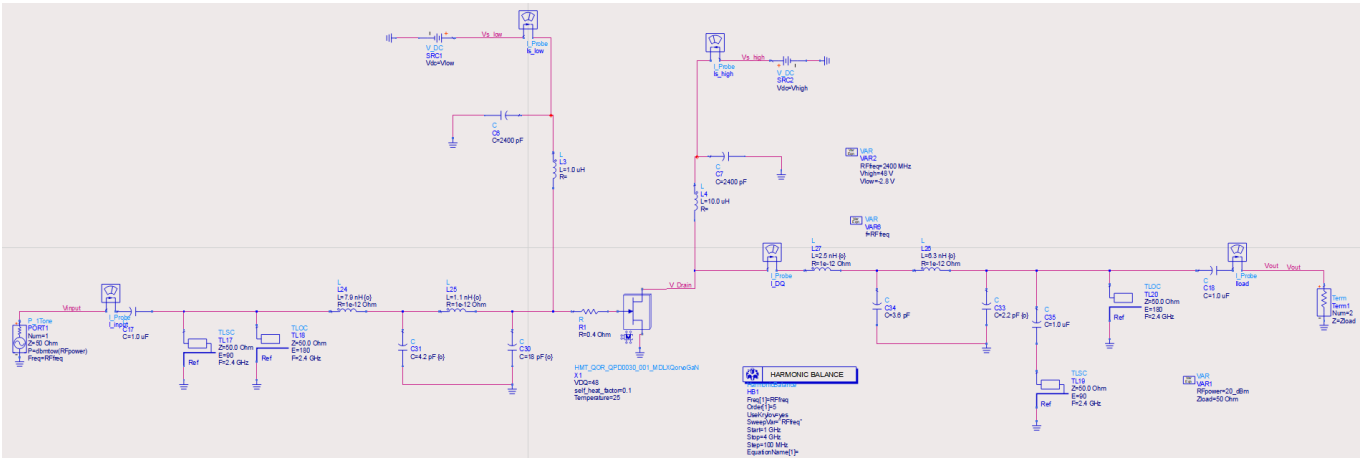


Fig 6.16: HB analysis (frequency Sweep) setup

Frequency Sweep (0-10 GHz): Obtained results show power output > 30dBm

Available Source Power dBm: 20.00

Fundamental Frequency	Fundamental Output Power dBm	Power Gain	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
1.000 G	-1.174	-21.17	-35.30	-70.24	-97.43	-150.7
1.100 G	-20.17	-40.17	-31.75	-81.28	-129.0	-177.9
1.200 G	-76.41	-96.41	-31.01	-131.7	-185.1	-268.6
1.300 G	-23.50	-43.50	-33.93	-72.29	-131.2	-200.6
1.400 G	4.930	-15.07	-52.63	-85.87	-135.9	-196.5
1.500 G	-8.738	-28.74	-32.65	-91.68	-121.8	-118.0
1.600 G	4.272	-15.73	-37.64	-82.31	-106.5	-121.0
1.700 G	15.97	-4.027	-42.05	-53.90	-95.73	-97.65
1.800 G	23.03	3.027	-69.30	-58.42	-115.3	-90.85
1.900 G	25.34	5.345	-39.96	-73.58	-97.87	-105.1
2.000 G	27.54	7.535	-50.66	-100.8	-108.6	-118.2
2.100 G	27.50	7.505	-56.97	-92.79	-133.0	-106.8
2.200 G	28.22	8.221	-65.76	-87.48	-94.60	-143.5
2.300 G	31.62	11.62	-75.46	-94.79	-87.79	-108.7
2.400 G	36.10	16.10	-64.98	-109.6	-78.88	-114.3

Fig 6.17: HB Analysis (frequency sweep) Results

Power Sweep (0-50 dBm input power): Amplifier output power saturated near 35 dBm with significant compression beyond 26 dBm power input, as observed:

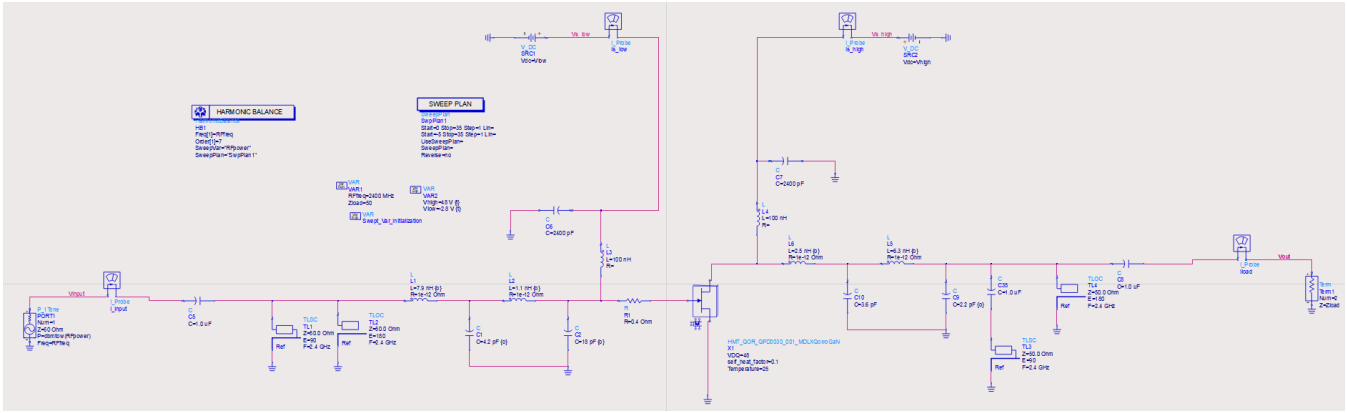


Fig 6.18: HB Analysis (power sweep) setup

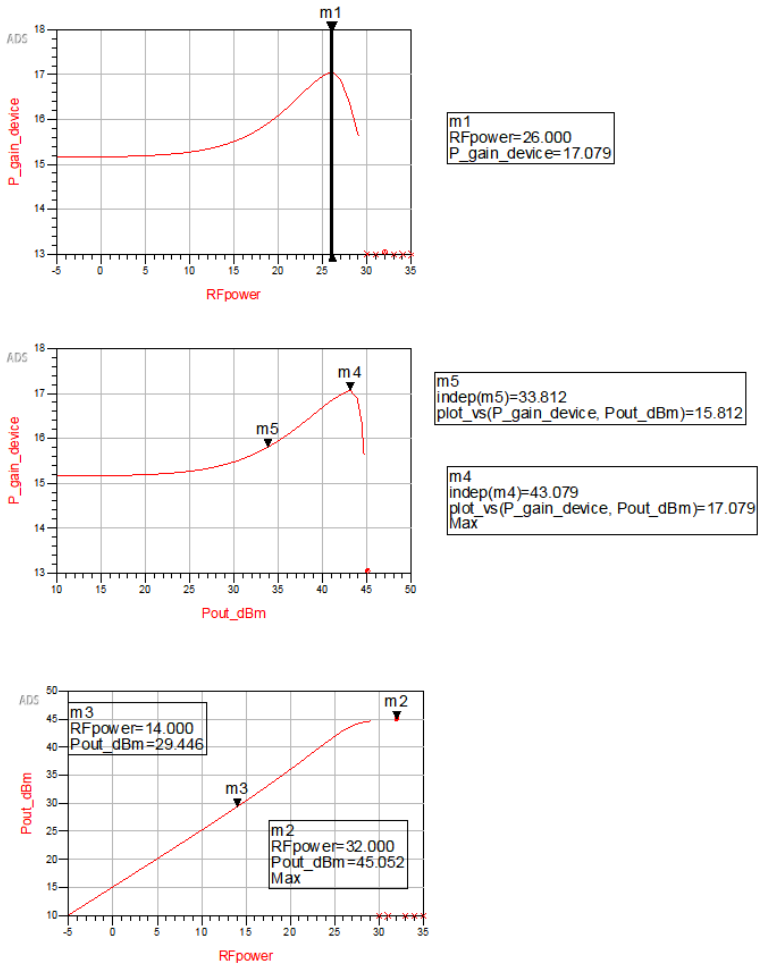


Fig 6.19: HB Analysis (power sweep) Results

One significant point to keep in mind is that till now, ideal components were used, which led to the above results. Now, we need to consider real-life component models which include parasitics and the above steps need to be re-analysed, after which, we can proceed with the layout.

6.8. Layout Design & Parasitic Considerations

The RF PCB layout is designed using a microstrip implementation with 35µm Cu traces on a 300µm FR4 substrate. This design accounts for harmonic stub placement, controlled impedance, lumped component port placement and via stitching for ground.

Modified network using parasitic models of all components involved, and wires and stubs converted to (modelled as) microstrip lines:

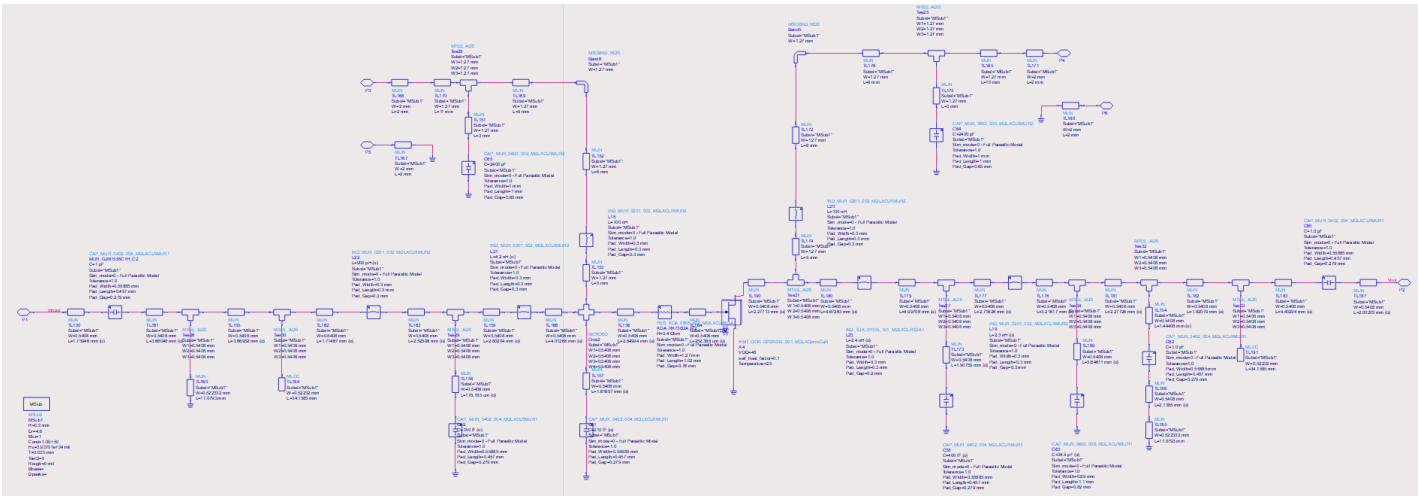


Fig 6.20: Overall network practical setup

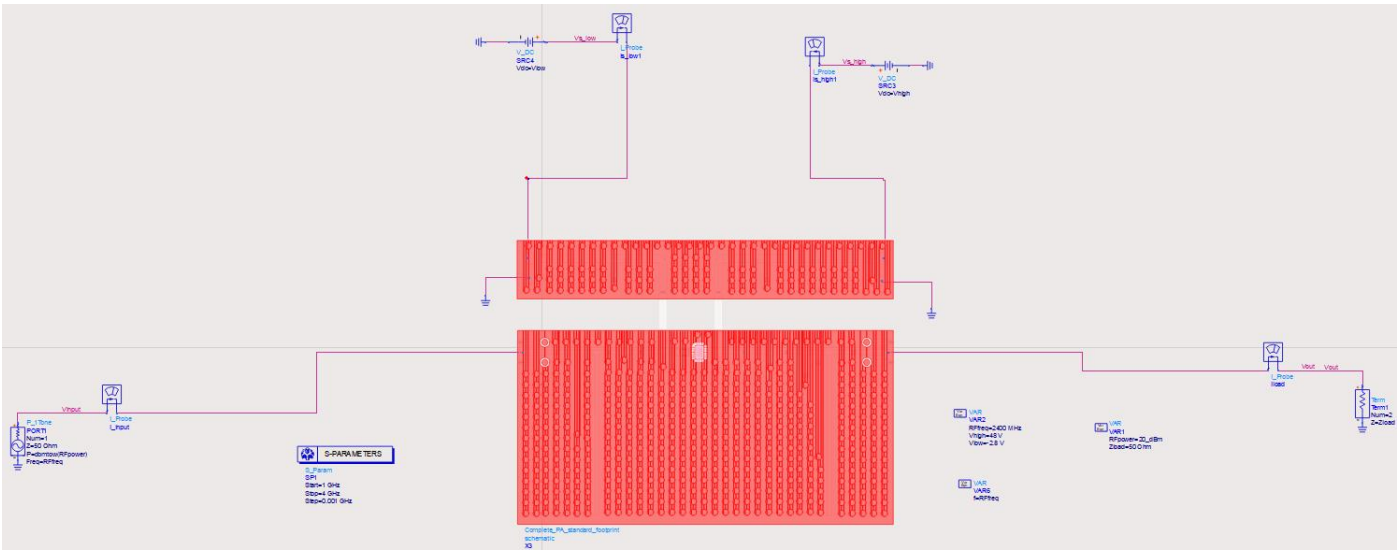


Fig 6.21: S-parameter analysis setup

S-Parameter anlaysis results:

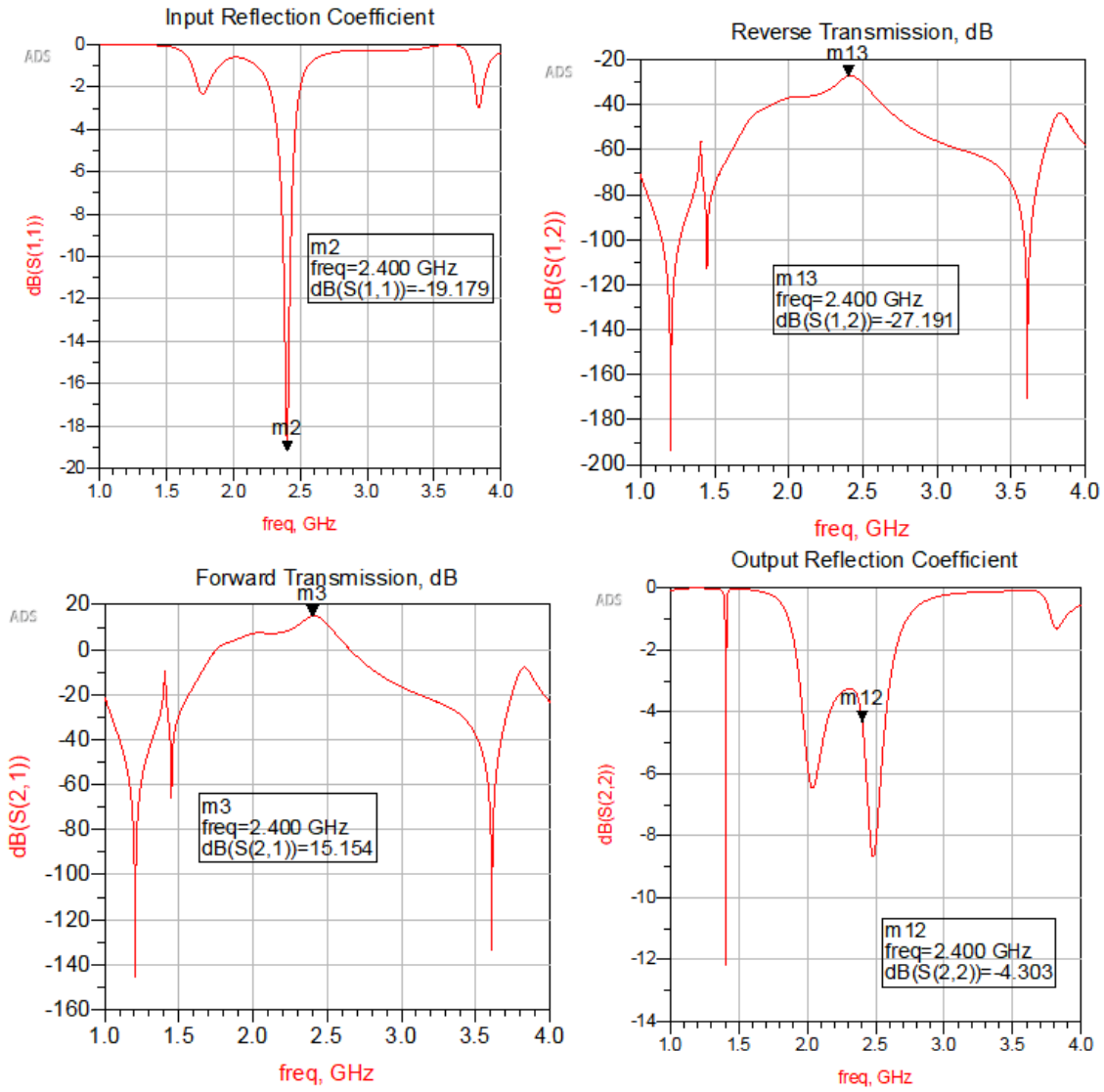


Fig 6.22: S-parameter analysis Results

Harmonic Balance analysis – Frequency Sweep

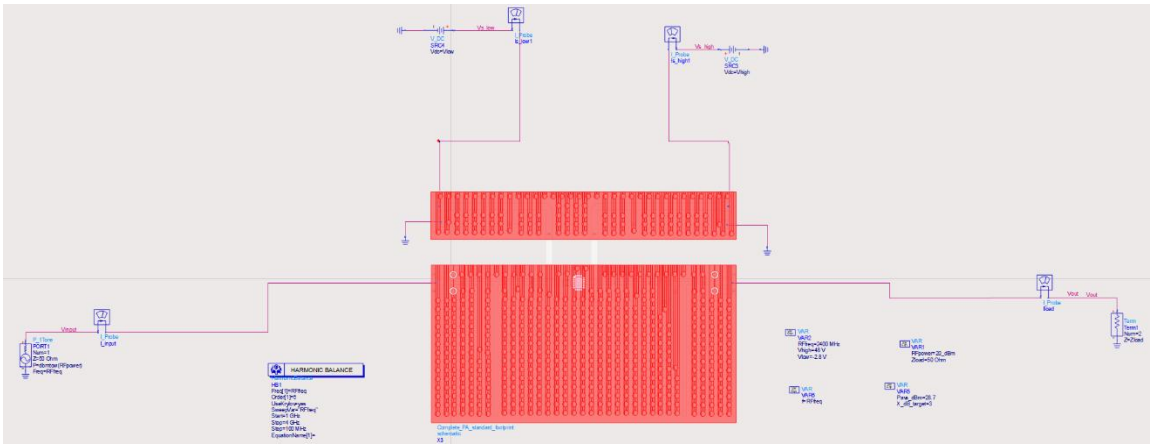


Fig 6.23: HB analysis (frequency sweep) setup

Available Source Power dBm: 20.00

Fundamental Frequency	Fundamental Output Power dBm	Power Gain	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
1.000 G	-1.174	-21.17	-35.30	-70.24	-97.43	-150.7
1.100 G	-20.17	-40.17	-31.75	-81.28	-129.0	-177.9
1.200 G	-76.41	-96.41	-31.01	-131.7	-185.1	-268.6
1.300 G	-23.50	-43.50	-33.93	-72.29	-131.2	-200.6
1.400 G	4.930	-15.07	-52.63	-85.87	-135.9	-196.5
1.500 G	-8.738	-28.74	-32.65	-91.68	-121.8	-118.0
1.600 G	4.272	-15.73	-37.64	-62.31	-106.5	-121.0
1.700 G	15.97	-4.027	-42.05	-53.90	-95.73	-97.65
1.800 G	23.03	3.027	-69.30	-58.42	-115.3	-90.85
1.900 G	25.34	5.345	-39.96	-73.58	-97.87	-105.1
2.000 G	27.54	7.535	-50.66	-100.8	-108.6	-118.2
2.100 G	27.50	7.505	-56.97	-92.79	-133.0	-106.8
2.200 G	28.22	8.221	-65.76	-87.48	-94.60	-143.5
2.300 G	31.62	11.62	-75.46	-94.79	-87.79	-108.7
2.400 G	36.10	16.10	-64.98	-109.6	-78.88	-114.3

Fig 6.24: HB analysis (frequency sweep) results

Power Sweep:

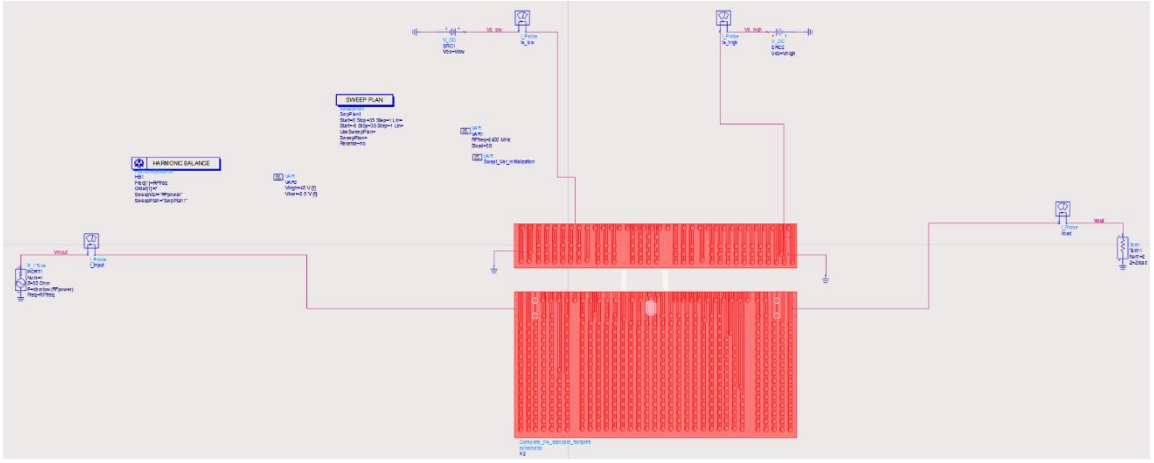


Fig 6.25: HB analysis (power sweep) setup

Results

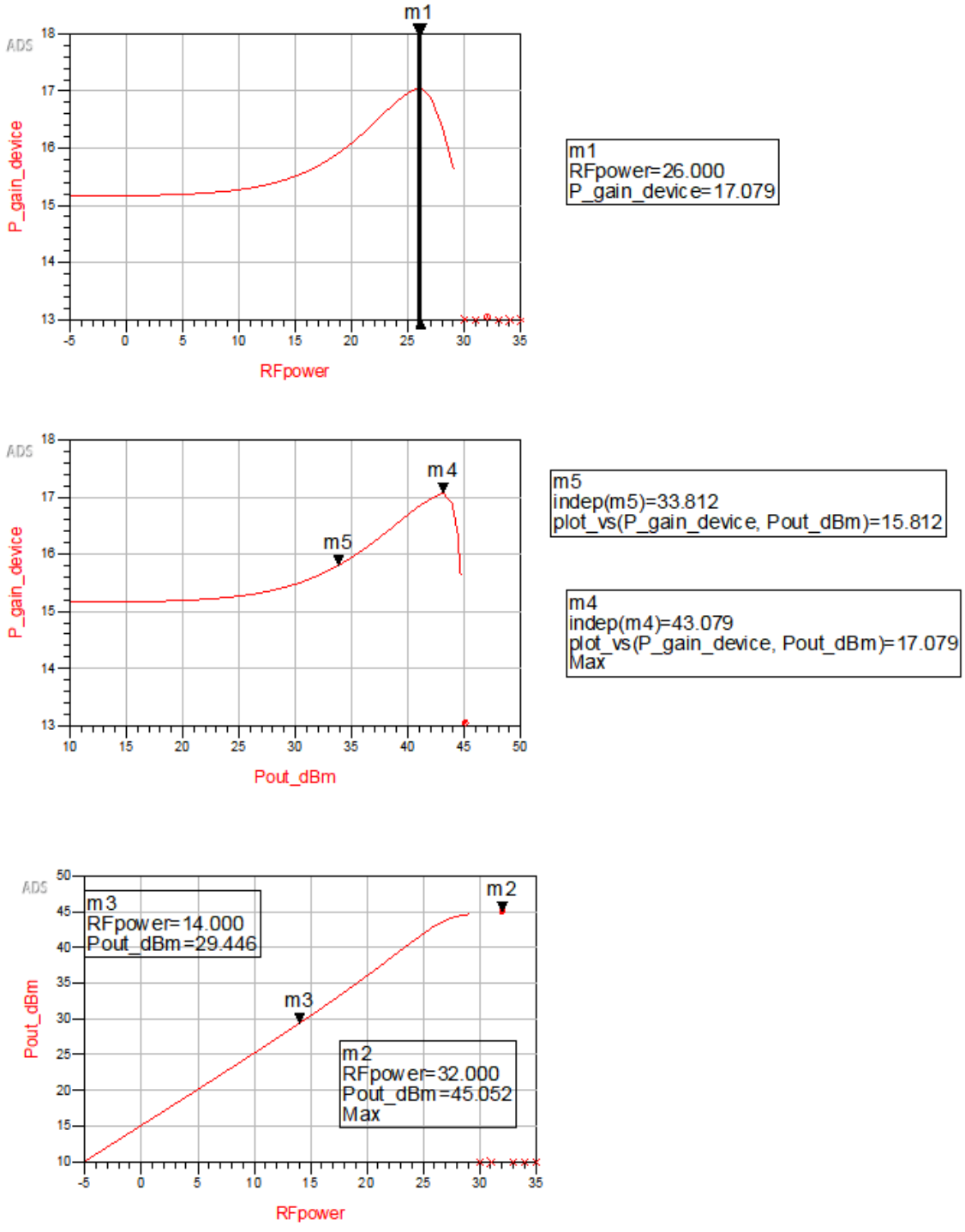


Fig 6.26: HB analysis (power sweep) results

PCB Layout design, without components:

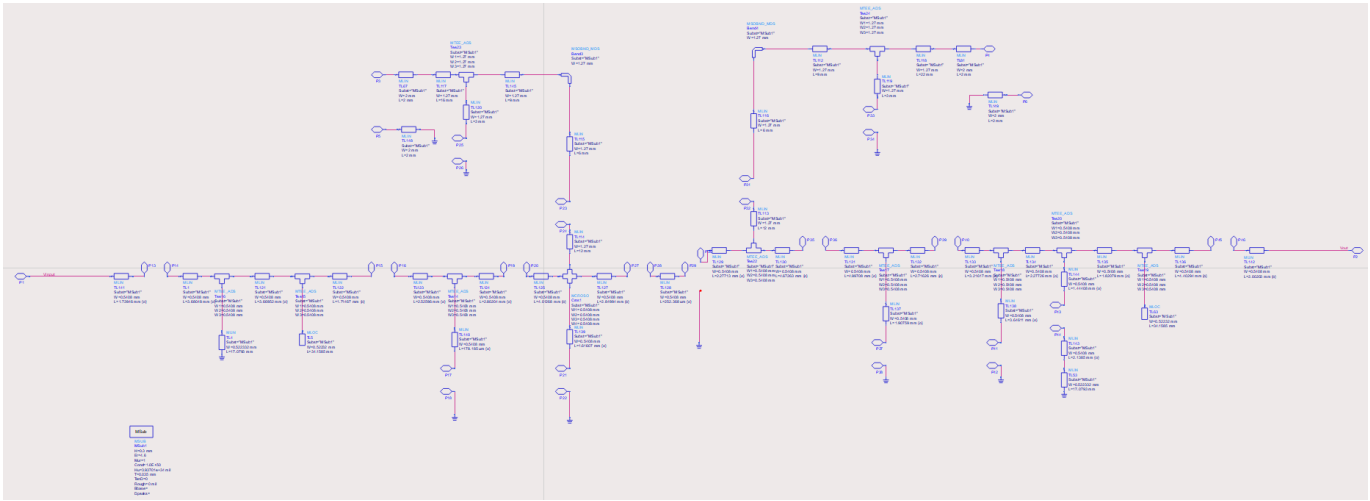


Fig 6.27: Network schematic without components (for layout)

PCB Layout:

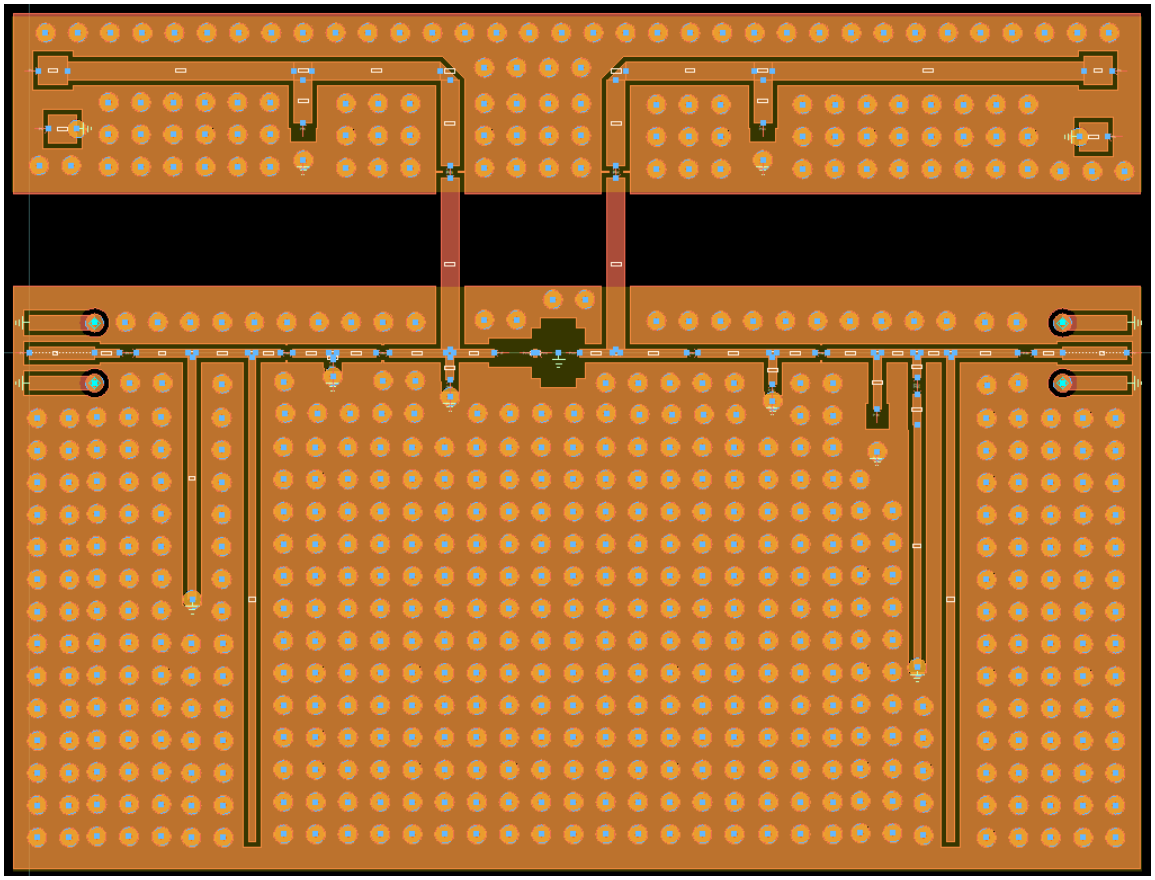


Fig 6.28: Designed PCB Layout

The dimensions of the designed PCB were measured as: ~8cm × 6cm

6.9. Summary of Obtained Results

The following table summarizes the obtained results, comparing them with the target specifications:

Parameter	**Design Specifications**	**Simulated Result**
Operating Frequency	2.4 GHz	2.4 GHz
Small Signal Gain (S_{21})	≥ 20 dBm	~15 dB
Output Power (P_{out})	≥ 35 dBm	36 dBm
Input Return Loss (S_{11})	< -10 dB	-19.2 dB
Stability (K, Δ)	Unconditionally Stable	Unconditionally Stable

Table 6.1.: Obtained Results Summary and Validation

7

Conclusion and Future scope

7.1. Conclusion

This work presents the complete design, simulation and layout development of a 2.4 GHz Class F Power Amplifier using a GaN HEMT device – specifically the QPD0030 from Qorvo. The amplifier was designed with the goal of achieving high efficiency and moderate power gain, ensuring a good power output, while operating within the ISM band, making it suitable for wireless communication applications such as Wi-Fi or industrial telemetry.

The design process began with an extensive review of device stability, confirming the unconditional stability of the QPD0030 transistor within the frequency band of interest. This was followed by load-pull simulations to determine optimal load impedances for maximizing output power and efficiency. DC I-V Characterization helped establish the load line and Q-point, which were essential in estimating the maximum power output capability.

Next, the input and output matching networks (IMN and OMN) were designed to transform the source and load impedances to the optimal values identified in the load-pull analysis. Smith chart techniques, harmonic tuning principles and transmission line synthesis were employed to ensure high-frequency performance and harmonic waveform shaping. The overall matching network was evaluated for gain and return loss across the band, and the design exhibited a peak power gain of approximately 20 dB, and subsequently ~15 dB – a reasonable value considering the chosen device and realistic component parasitics.

Harmonic Balance simulations were carried out for both frequency and power sweeps, confirming the amplifier's ability to deliver sufficient output power with non-linear efficiency benefits. S-parameter analysis of the complete network validated the performance in terms of reflection and transmission characteristics, indicating well-matched ports and appropriate bandwidth behaviour.

The layout was meticulously designed by considering the RF PCB Design principles, including via placement, transmission line sizing and decoupling strategies. A key learning during the layout process was the importance of careful

component selection among various vendors, accounting for parasitics SMD pad effects and manufacturing tolerances. Additionally, the necessity of providing separate RF and DC grounds was observed, which improved isolation and performance by reducing noise coupling and interference – an essential insight for real-world implementations.

Although the final gain achieved was slightly lower than theoretical predictions, the overall design demonstrates a stable, realizable and efficient amplifier suitable for prototyping or integration into communication front-ends.

7.2. Future Scope

While the current design provides a functional 2.4 GHz Class F amplifier, several avenues exist for enhancement and further exploration:

- Higher Efficiency and Gain Optimization:

  Future iterations can explore advanced harmonic terminations, including third harmonic peaking and waveform engineering, to push efficiency beyond current values. Utilizing more advanced GaN HEMTs with higher gain-bandwidth products or tailored Class F configurations may also yield improvements

- Thermal and Packaging Considerations:

  Including thermal analysis in the design cycle can enhance the reliability for high-power applications. Integrating proper heat-sinks, thermal vias and using low-loss substrates like Rogers could improve both performance and ruggedness.

- Bias Network Automation and Protection:

  The bias circuitry can be refined using adaptive bias controllers or current sensors to improve robustness under varying load conditions or input drive levels.

- Fabrication and Measurement:

  The fabricated layout can be tested using a Vector Network Analyzer (VNA), power meter, and spectrum analyser to validate simulated performance. Differences between EM co-simulated and measured data will reveal important practical effects for refinement.

- System-Level Integration:

  This amplifier can be incorporated into practical wireless systems such as:

  - Wi-Fi routers or IoT Gateways for extended range
  - Industrial RF Telemetry or RF identification Systems
  - RF front-ends of drone communication modules

- Miniaturization and Multi-band support:

  The same design methodology can be extended to multi band or broadband PAs, especially using MMIC approaches or with the help of tunable components for reconfigurable networks.

In conclusion, this project forms a strong foundation in high-frequency PA design using GaN Technology, and demonstrates how simulation-driven RF development can yield realizable hardware. The experience and insights gained through this work contribute not only to academic growth but also to real-world RF product development.

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